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Inkjet-Printed Zinc Tin Oxide Thin-Film Transistor

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Recently, there has been considerable interest in adapting printing approaches that are typically used in the graphic arts to the printing of electronic circuits and circuit components. We report the fabrication of solution-processed oxide transistors using inkjet printing. A zinc tin oxide sol−gel precursor is utilized as the ink for directly printing a thin uniform semiconducting layer. The printed device performance is significantly influenced by printing conditions such as the surface wettability and substrate temperature. The inkjet-printed transistors exhibit reproducible electrical performance, demonstrating their potential application in low-cost manufacturing of large-area flat panel displays.

Introduction

Zinc oxide (ZnO) is a direct wide band gap semiconductor ($E_g = 3.37$ eV) and is therefore an excellent candidate for UV light-emitting diodes (LEDs), lasers, and transparent transistors.[1−5] The conduction band of ZnO is primarily composed of large, metal-based 4s orbitals that spread out spatially with isotropic shapes such that direct overlap between neighboring metal orbitals is possible.[6,7] The unique properties of the conduction band have led to recent interest in using ZnO as a channel material for thin-film transistors (TFTs) and as a replacement for conventional Si-based materials[8,9] and organic semiconductors.[10,11] The majority of current high-performance TFTs consist of either low-temperature polycrystalline Si (LTPS) or hydrogenated amorphous silicon (a:Si-H). Both of these Si-based thin films are difficult to fabricate with solution processes such as spin coating and inkjet printing that allow for economical manufacturing of TFTs.

Spin coating is a solution-based process used for depositing thin films and has been employed in the fabrication of solution-processed oxide semiconductor transistors consisting of ZnO colloidal dispersions or sol−gel solutions.[12,13] However, spin coating requires an additional patterning procedure for achieving selective deposition and also wastes a large fraction of material. With this in mind, we have sought to apply inkjet printing technology to the deposition of solution-processed oxide semiconducting layers. Inkjet printing is an attractive technique for direct writing of patterns and the delivery of precise quantities of materials because it circumvents the need for conventional photolithography and vacuum deposition methods.[14,15] In particular, inkjet printing is amenable to selective deposition of semiconducting layers for large-area printed transistors.[16] Inkjet-printed, organic semiconductor-based thin-film transistors have been extensively reported in the literature. In these reports, inkjet printing conditions such as ink solvent types and substrate properties critically influence the crystallinity and molecular arrangement of the organic semiconductors.[17] However, inkjet-printed ZnO-based semiconductors have been examined only in recent work.[18,19]

Recently, a new set of ZnO-based materials has been investigated for use in amorphous oxide transparent TFTs that exhibit reproducible device performance with a high degree of uniformity.[5] Most research has focused on indium zinc oxide (IZO) and gallium indium zinc oxide (GIZO). However, little work has been conducted on zinc tin oxide (ZTO) except for the recent study by Chang et al. They have shown that ZTO produces good transistor characteristics, but their synthesis method includes chlorides as starting materials, which can leave behind toxic byproduct.[20] In our previous study, we synthesized a sol−gel derived ZTO precursor solution using a different precursor and demonstrated spin-coated amorphous semiconductor TFTs with good electrical performance.[21]

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In this article, we demonstrate that interfacial energetic compatibility of the semiconductor ink with the dielectric−electrode surfaces plays a vital role in forming coherent heterogeneous interfaces. Printing of the ink on the dielectric−electrode surfaces results in the formation of the semiconductor channel between electrodes on top of the dielectric surface. We first report the importance of the uniform spatial distribution of the solute during ink drying in achieving underlying coherent interfaces between the semiconductor and electrode and/or the semiconductor and dielectric where charge injection and charge accumulation occur. The transistor performance is largely dependent on the quality of such heterogeneous interfaces. Interfacial energies and drying conditions should be carefully controlled to yield the high-quality coherent interfaces. We investigate the influences of surface wettability and the preprinting substrate temperature on the electrical performance of the inkjet-printed transistors.

Experimental Section

The ink solution for printing the zinc tin oxide (ZTO) semiconductor was prepared by dissolving zinc acetate dihydrate [$Zn(CH_3COO)_2 \cdot 2H_2O$, >98%, Aldrich] and tin(IV) acetate [$Sn(CH_3COO)_2$, Aldrich] in 2-methoxyethanol (99.8%, anhydrous, Aldrich). The concentration of metal precursors was 0.75 M, and the molar ratio [Sn/(Sn + Zn)] was 0.3. Ethanolamine (≥99%, Aldrich) was used as a stabilizing agent to improve the solubility of the precursor salts. Prior to inkjet printing, the formulated solution was stirred for 12 h at room temperature and filtered through a 0.2 μm PTFE (polytetrafluoroethylene) membrane filter (diameter of 13 mm, Whatman). The ink viscosity was 17.8 mPa s at a shear rate of 50 s^{-1}, as measured by a cone and plate viscometer (DV-III+, Brookfield Engineering). The printer setup consisted of a drop-on-demand (DOD) piezoelectric inkjet nozzle (orifice size of 50 μm) manufactured by MicroFab Technologies, Inc. (Plano, TX). The print head was mounted on a computer-controlled three-axis gantry system with a movement accuracy of ±5 μm. The gap between the nozzle and the surface was maintained at ∼0.5 mm during the printing process. Uniform droplet ejection was achieved by applying a 15 μs, 60 V pulse at a frequency of 1000 Hz. A heavily doped Si wafer with a thermally grown 200 nm thick SiO_2 layer (capacitance of ∼16.8 nF cm^{-2}) was used as a dielectric/common gate electrode.

We fabricated coplanar-type transistors by either inkjet printing or spin coating the ZTO ink between ITO source and drain electrodes. A patterned ITO electrode was prepared in the following manner: (1) standard photolithography on top of an n^+ Si substrate with a 200 nm thick SiO_2 layer, (2) sputtering ITO, (3) performing a lift-off method, and (4) annealing the patterned ITO at 350 °C. The width and length of the channel were 100 and 10 μm, respectively. To investigate the variation in printed morphology as a function of wettability, the substrates with patterned ITO electrodes were either cleaned with isopropyl alcohol (IPA, 99.5%, Ducksan Co., Ltd., denoted IPA-cleaned) or treated with hexamethyldisilazane (97%, Aldrich, denoted HMDS-treated). Before the HMDS treatment, the surface of the thermally grown SiO_2 was cleaned with H_2SO_4/H_2O_2 to form a self-assembled monolayer. A single droplet of ZTO ink with a volume of 30 pL was printed onto both the IPA-cleaned and HMDS-treated substrates at either 50 or 80 °C, while the ink was spin coated at 3000 rpm for 20 s on the IPA-cleaned substrate at 25 °C. The resulting ZTO layers were dried at 95 °C for 90 s to evaporate the solvent and annealed at 500 °C in air for complete thermal decomposition of organic residues and metal salts. Two-dimensional morphologies and surface profiles of the printed patterns were obtained with a surface profiler (Dektak 150, Veeco Instruments Inc.). A postannealing step was then performed at 200 °C under a H_2/N_2 atmosphere to improve the electrical performance of the transistor prior to measurement. $I-V$ characteristics for all transistors were measured in air using an Agilent 4155C semiconductor parameter analyzer to assess the electrical performance of the transistors.

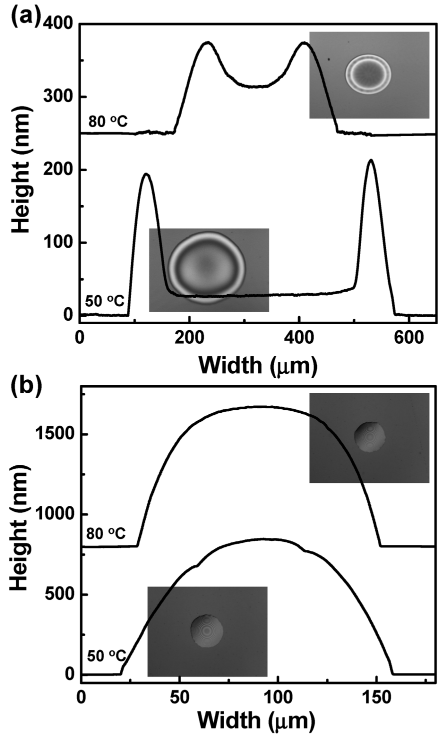

Figure 1. Two-dimensional profiles of the inkjet-printed ZTO single dot: (a) on the IPA-cleaned SiO_2/n^+ Si substrate at 50 and 80 °C and (b) on the HMDS-treated SiO_2/n^+ Si substrate at 50 and 80 °C. Insets show the optical images of the corresponding single dots.

Results and Discussion

The IPA-cleaned SiO_2/n^+ Si substrate was preheated to either 50 or 80 °C prior to inkjet printing of a single droplet of the ZTO sol−gel solution. At 50 °C, a dot-shaped deposit resulted with significant fluctuation in thickness, the so-called "coffee-ring pattern", as shown in Figure 1a. The diameter of the dot was 490 μm, and the peak-to-valley height ratio was ∼170 nm. Increasing the substrate temperature led to the formation of dot-shaped patterns smaller in size with better uniformity. The dot diameter was ∼300 μm at 80 °C, and the peak-to-valley height ratio was 60 nm. Since 2-methoxyethanol has a low surface tension (31.8 mN/m), the sol−gel ink wets well on an IPA-cleaned SiO_2/n^+ Si surface (contact angle of < 5°) (see Figure S1 of the Supporting Information). The droplet spreads out significantly upon contacting the substrate and is subsequently pinned at the contact line. Complex hydrodynamic flows can develop if the evaporating droplet is composed of multiple solvents. It is believed that both the convective flow and the composition gradient-driven Marangoni flow are outwardly induced from the center to the edge in sol−gel ink droplets, which segregates the solute at the contact line.[17,22−25] The coffee-ring effect can be suppressed if the solvents rapidly evaporate prior to the onset of hydrodynamic flows, which is accomplished by heating the substrate. As seen in Figure 1a, increasing the preprint temperature of the substrate from 50 to 80 °C inhibits the segregation

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phenomenon to some extent but does not completely eliminate it. Further increasing the substrate temperature is undesirable because the jetting would become unstable due to premature evaporation at the orifice as a result of the short nozzle−substrate distance.

Modification of the surface energy gives rise to markedly different deposit patterns. The evaporation of droplets placed on an HMDS-treated SiO_2/n^+ Si substrate leads to a dome-shaped deposit (height of 850 nm and width of 140 μm at 50 °C) without the coffee-ring effect (Figure 1b). Smaller dome-shaped patterns with slightly higher aspect ratios were obtained with an increase in the substrate preprint temperature. An ink droplet placed on the HMDS-treated SiO_2 and ITO surfaces retains a hemispherical shape with a high contact angle (~46°) (see Figure S1c,d of the Supporting Information). The presence of thicker liquid layers at the contact line permits uniform slow evaporation to occur throughout the liquid−gas interface. In such a case, the contact line is not pinned and instead retracts as the droplet shrinks, maintaining a hemispherical shape.[25,26] As the solvent slowly evaporates, the solutes suspended in the evaporating droplet are gradually concentrated, forming a dome-shaped deposit without segregation.

We fabricated the transistors using a bottom-gate, bottom-contact structural configuration by inkjet printing the ZTO sol−gel solution on either an IPA-cleaned or HMDS-cleaned surface (see Figure S2a of the Supporting Information). The surfaces were preheated to either 50 or 80 °C, and their optical images are shown in Figure S2b−e. The inkjet-printed, as-dried layers were then subjected to further annealing in air at 500 °C to remove organic species and to decompose the metal salt. The resulting ZTO films are composed of an amorphous phase in which ~1−2 nm sized particles of Zn_2SnO_4 are embedded as confirmed by HRTEM and XRD.[21] We observed significant differences in the device performance as a function of the substrate wettability and the preheat temperature as shown in Figure 2a. The detailed electrical performance parameters such as saturation mobility, threshold voltage, on/off current ratio, and subthreshold slope are extracted from the transfer curves at a drain voltage of 20 V and are summarized in Table 1.

The performance of the inkjet-printed devices on the IPA-cleaned surfaces significantly depends on how well the channel layer is formed between the source and drain electrodes. The device parameters fluctuate when the printed dot position is off-center; this creates nonuniformity in the channel layer, and the thick region of the circular film is deposited across the electrodes as shown in Figure 3. Even in the case of uniform channel formation, the thickness of the printed material is also a critical factor for the transistor. When printed on substrates preheated to 50 °C, the droplet spreads out more than in the 80 °C case, forming a larger printed circular dot in which a thinner channel (~25 nm) forms between the electrodes. In contrast, the device printed on the substrate preheated to 80 °C shows superior performance versus the one printed at 50 °C (Figure 2a and Table 1). The mobility and on current of the TFTs inkjet printed at 80 °C were 0.58 $cm^2\ V^{-1}\ s^{-1}$ and 6×10^{-5} A, respectively, and were slightly lower for the 50 °C case (0.30 $cm^2\ V^{-1}\ s^{-1}$ and 3×10^{-5} A, respectively). This difference in electrical performance is attributed to the variation in ZTO active layer thickness (the thicknesses at 50 and 80 °C were 25 and 50 nm, respectively). Kim et al. observed similar results in which the thickness of

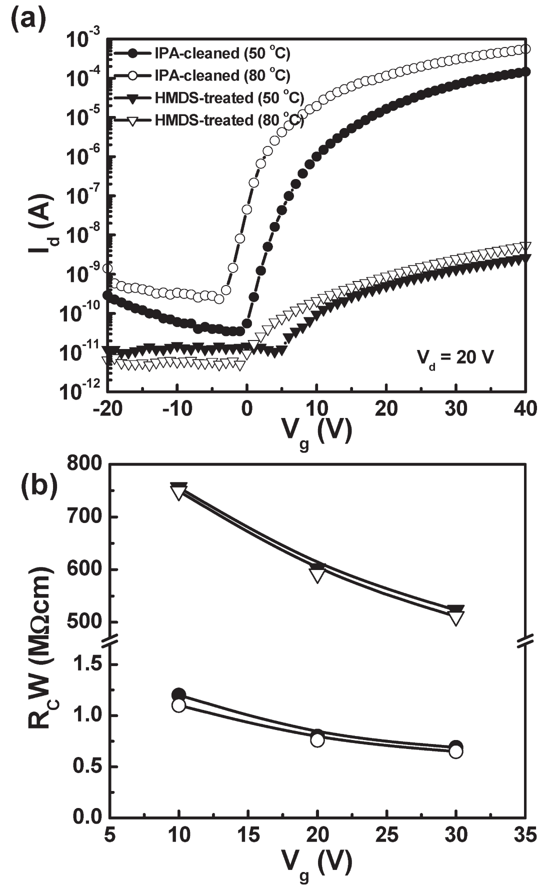

Figure 2. (a) Transfer characteristics of an inkjet-printed transistor fabricated under different surface conditions as a function of the preheated substrate temperature. (b) Channel width-normalized contact resistance of the devices fabricated under different surface conditions and at substrate temperatures. The contact resistance was obtained by means of the transmission line method (TLM), which was plotted as a function of the channel length.

solution-processed oxide semiconductor plays an important role in determining the mobility and current level.[27] The coplanar-type spin-coated counterpart with the 30 nm thick channel layer exhibits slightly inferior performance compared to that of the inkjet-printed ZTO at 80 °C as shown in Figure 4 and Table 1. To confirm the influence of the film thickness on the performance of devices, we fabricated the spin-coated devices with different active layer thicknesses by control of the number of coatings. The TFT with a 50 nm thick channel exhibits a mobility of 0.60 $cm^2\ V^{-1}\ s^{-1}$, whereas a similar mobility of 0.57 $cm^2\ V^{-1}\ s^{-1}$ is observed for the device with a 80 nm thick channel (see Figure S3 of the Supporting Information). This means that the sol−gel derived ZTO active layer has an optimal film thickness of ~40−50 nm. The off current increases proportionally with active layer thickness, but the mobility and the on current reach a maximum since the effective channel thickness is fixed.

The performance of the inkjet-printed devices is also significantly influenced by the surface wettability. The transistors printed on the HMDS-treated surfaces show extremely inferior electrical performance compared to those printed on the IPA-cleaned surfaces even though the channel layer is sufficiently thick (~850 nm) (see Figure 2a). The mobility and on current are 0.003 $cm^2\ V^{-1}\ s^{-1}$ and 3×10^{-9} A at the preheat temperature of 50 °C and 0.016 $cm^2\ V^{-1}\ s^{-1}$ and 5×10^{-9} A at 80 °C, respectively. Furthermore, some evidence of contact-limited performance, as characterized by the concave down regions in the

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Table 1. Electrical Performance Parameters for the Inkjet-Printed and Spin-Coated ZTO Transistors Fabricated under Different Surface Wetting and Substrate Temperature Conditions

fabrication method	substrate treatment	substrate temperature (°C)	mobility ($cm^2\ V^{-1}\ s^{-1}$)	threshold voltage (V)	on current (A)	on/off current ratio	subthreshold slope (V/decade)
inkjet-printed	IPA-cleaned	50	0.30	2.2	3×10^{-5}	4×10^{6}	1.53
		80	0.58	1.9	6×10^{-5}	5×10^{6}	1.38
	HMDS-treated	50	0.003	1.2	3×10^{-9}	3×10^{2}	5.45
		80	0.016	0.5	5×10^{-9}	1×10^{4}	4.15
spin-coated	IPA-cleaned	25	0.32	1.3	3×10^{-5}	1×10^{6}	1.56

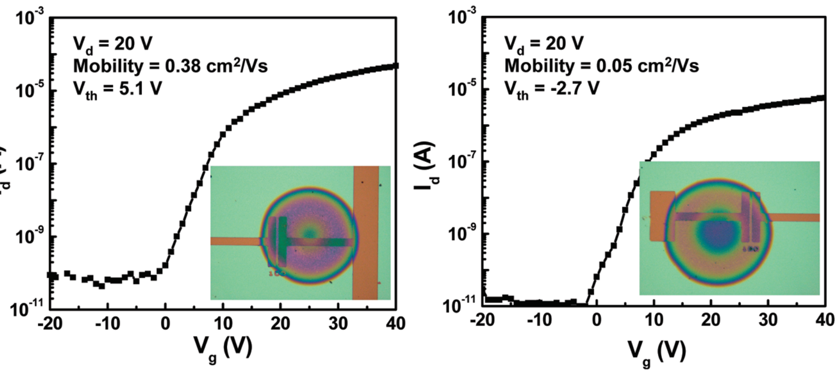

Figure 3. Transfer characteristics and electrical parameters of the inkjet-printed transistors. The device performance depends on the location of the ZTO dot with respect to the center of ITO source and drain electrodes. Inkjet printing was performed on the IPA-cleaned substrate at 80 °C.

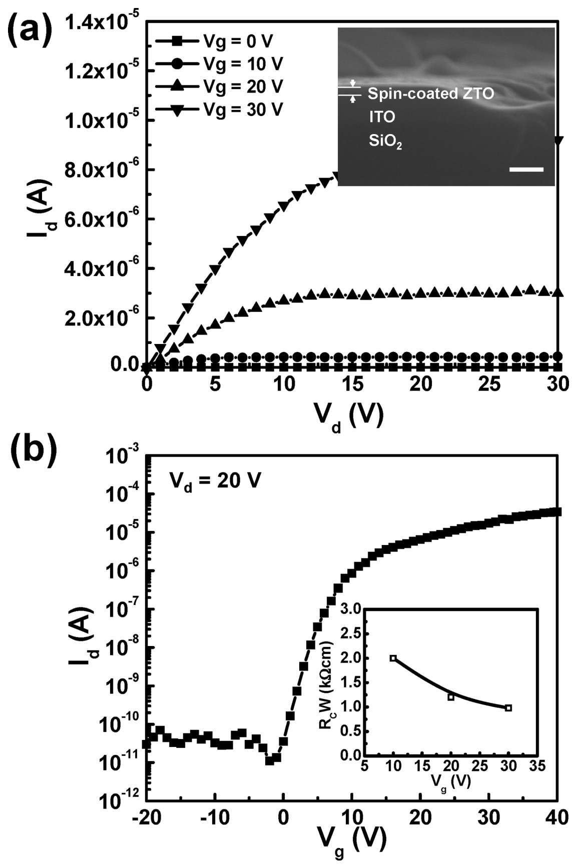

Figure 4. (a) Output and (b) transfer characteristics of the coplanar-type spin-coated ZTO TFT. The inset in panel a shows a cross-sectional SEM view of the spin-coated ZTO layer. The scale bar is 100 nm. The inset in panel b shows the channel width-normalized contact resistance (R_cW) as a function of gate voltage.

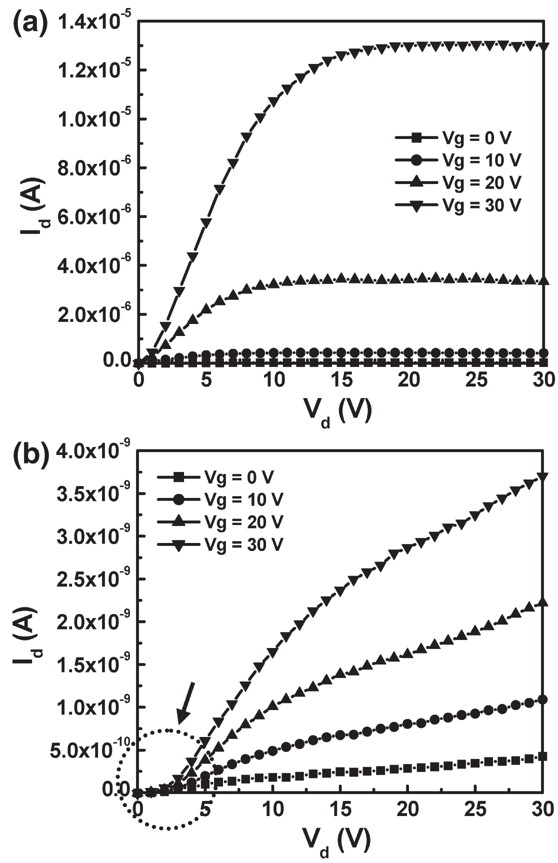

Figure 5. Output characteristics of the inkjet-printed ZTO TFTs fabricated on (a) IPA-cleaned and (b) HMDS-treated surfaces. The substrate temperature was 80 °C. Output characteristics of the inkjet-printed TFTs on IPA-cleaned substrates show good saturation performance, while the inkjet-printed TFTs on HMDS-treated substrates show the existence of contact resistance in the low drain voltage regime.

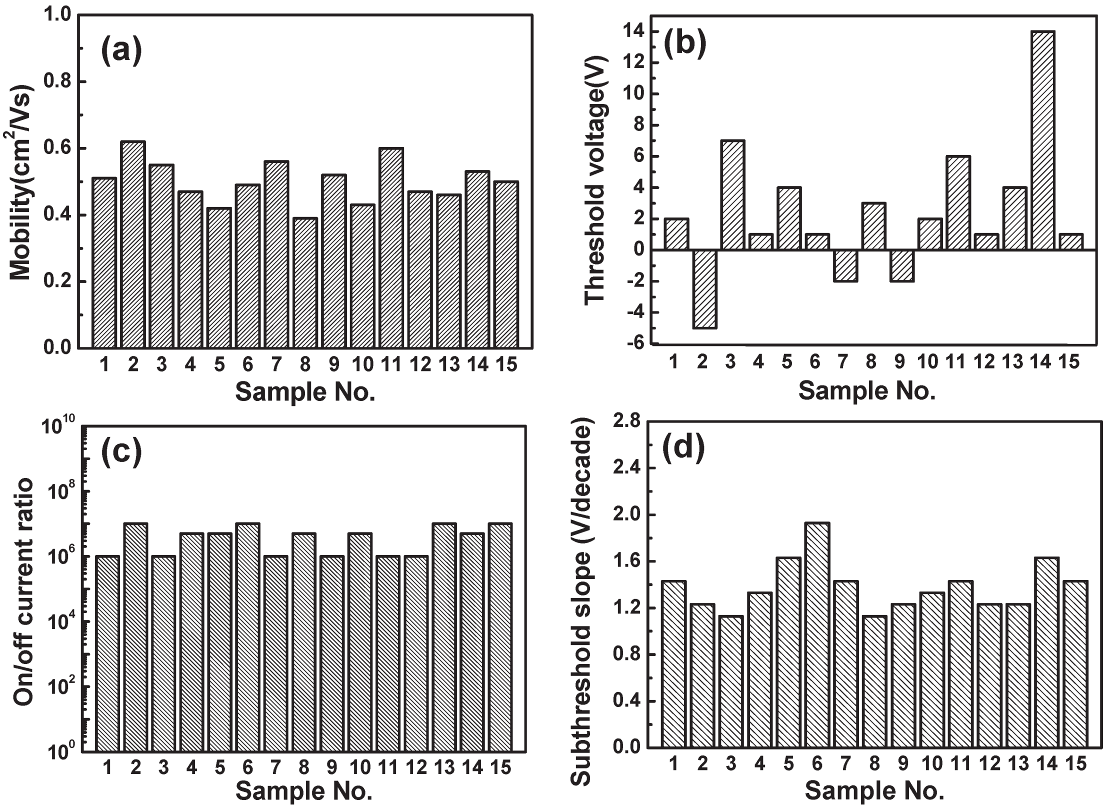

Figure 6. Selected device performance for the inkjet-printed ZTO 20 × 20 array in 1 cm × 1 cm (unit size of 500 μm × 500 μm).

low source-drain bias regime, indicates a nonohmic contact at the ITO−ZTO interface (Figure 5b). In contrast, the contact resistance seems to be low for both the inkjet-printed transistors on IPA-cleaned surfaces (Figure 5a) and the spin-coated device (Figure 4). This observation leads us to speculate that a contact problem exists at the interfaces between the semiconducting layer and the electrode in the devices printed on the HMDS-treated surfaces.

The interfacial problem at the semiconducting layer−electrode interfaces originates from the hindrance of charge carrier injection, which is manifested by a large contact resistance and causes poor device performance. The channel width-normalized contact resistance (R_cW) obtained from the transmission line method (TLM) analysis as a function of gate voltage is plotted in Figure 2b. For the TFTs printed on the HMDS-treated surfaces, the contact resistances varied from 500 to 750 kΩ cm as the gate voltage was increased from 10 to 30 V. These values are much larger than those obtained for the inkjet-printed transistors on IPA-cleaned surfaces (0.6−1 kΩ cm), which is similar to that of the spin-coated device (1−2 kΩ cm) (Figure 4b). The contact resistance values correlate well with the observed variations in device performance (Figure 2a).

Charge carrier injection can be hindered by either the formation of physically incoherent interfaces or heterogeneous electronic energy-level mismatch between the active layer and the source and drain electrodes. Since the HMDS-coated ITO electrode is reported to have a work function of ∼4.3−5.2 eV, it is expected to be energetically well-matched with the ZTO semiconductor (work function of ∼4.5 eV) and should allow for the formation of a low-contact resistance interface.[28,29] Hence, the heterogeneous energetic mismatch can be ruled out as the cause of the large contact resistance. The cross sections of the semiconductor−electrode interfaces were directly observed by SEM to investigate the physical morphology present at the interface. The ZTO semiconducting layer printed on the IPA-cleaned surfaces shows a coherent interface for both the ITO electrode and the SiO_2 dielectric (see Figure S4 of the Supporting Information). In contrast, the film printed on the HMDS-treated surfaces forms an incoherent interface containing many large pores. In particular, the large pores were observed at the interface between the ZTO active layer and the HMDS-treated ITO source and drain electrodes rather than at the interface with the SiO_2 dielectric. This microstructural evidence clearly supports the notion that the large contact resistance results from the formation of a physically incoherent interface. The contact resistance in a TFT with a bottom contact configuration is mainly determined by the interfacial quality of the active layer faced with electrodes, not by that with the dielectric.

The use of hydrophobic SAMs such as HMDS is an effective way to modify the dielectric surface and to remove undesirable charge trap sites and moisture. In addition, the presence of SAMs may assist with molecular ordering and crystallization of the overlying organic semiconductors and provide good semiconductor−electrode energy-level alignment for efficient charge transport and injection.[30,31] However, the electrical performance of ZnO-based amorphous oxide semiconductors is insensitive to atomic ordering and lattice matching at the interfaces, and the sol−gel derived film requires high-temperature annealing (500 °C) that will likely decompose the organic SAM molecules (at ∼300−400 °C). There was no difference in the crystallinity of

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ZTO as coated on either HMDS- or IPA-treated substrates, and both films were amorphous as confirmed by XRD analysis. The HMDS treatment appears to have an adverse affect in printed oxide-based transistors. When nonwetting semiconducting ink is printed on surfaces with which it has a high contact angle, air is likely trapped at the step between the ITO electrode and the SiO_2 dielectric as the ink is rapidly placed and dried, which in turn leads to incoherent interface formation. During the inkjet printing, the interfacial energies must be carefully controlled such that the ink wets well on both the electrode and the dielectric surfaces. Our observations clearly indicate that the surface energy and the substrate temperature play an important role in the formation of coherent interfaces and uniform channel layers between the electrodes, which in turn affects the device performance. Under well-controlled conditions, we successfully fabricated a printed TFT array that gave consistent device parameters as shown in Figure 6 (mobility of 0.58 ± 0.1 $cm^2\,V^{-1}\,s^{-1}$, threshold voltage of 1.9 ± 3.5 V, and subthreshold slope of 1.38 ± 0.21 V/decade).

Conclusions

We have demonstrated the inkjet printing of oxide semiconductors in transistors with electrical performances comparable to those of amorphous Si-based transistors. The printed transistor performance is extremely dependent on both the film morphology and the quality of the semiconductor−electrode and/or semiconductor−dielectric interfaces. The semiconductor ink should be stably jetted for accurate deposition at the center of the source and drain electrodes and should wet well the surfaces of the electrode and the dielectric for the achievement of coherent heterogeneous interfaces. Drying of the printed ink droplet should also be controlled by preheating the substrate to ensure the formation of a homogeneous and uniform channel layer with the optimum thickness. The consistent and reliable electrical performance of the inkjet-printed zinc tin oxide transistor array demonstrates the potential of such devices for application in the low-cost manufacturing of large-area flat panel displays, including liquid crystal displays (LCDs) and organic light-emitting diodes (OLEDs).

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Supporting Information Available: Contact angles of a sessile drop of ZTO ink on various substrates (Figure S1), schematics and optical images of the fabricated TFTs (Figure S2), transfer characteristics of the spin-coated ZTO TFTs (Figure S3), and SEM images of cross sections of the channel region in the inkjet-printed ZTO TFTs (Figure S4). This material is available free of charge via the Internet at http://pubs.acs.org.