

Operations and Maintenance Manual

Computerized Pavement Condition Survey Unit

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16. Abstract <p>A computerized field pavement condition survey unit and an IBM PC/XT computer base office reader and analysis system were developed for use in the pavement management program used by WSDOT.</p> <p>The pavement condition recording and computing device is a microprocessor controlled, data acquisition and reduction system which uses a combination of manual inputs and odometer readings to develop pavement condition reports. These reports are printed on the system printer and written to a standard compact magnetic tape cartridge along with the raw data for later inclusion in the Washington State Department of Transportation's pavement management data base.</p> <p>The device, including all of its attendant equipment, is fully portable so that it may be used in any motor vehicle that has an odometer pulse generator (preferably producing approximately 4,000 TTL level counts per mile) and 12 Vdc power source.</p> <p>The office system consists of an IBM PC/XT or AT microcomputer with a printer and a 20 megabyte cartridge tape drive. It also has the software needed to read, preview, analyze and convert the data for direct entry into WSDOT's pavement management system.</p>					
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**OPERATIONS AND MAINTENANCE MANUAL
COMPUTERIZED PAVEMENT CONDITION
SURVEY UNIT**

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FINAL REPORT

OPERATIONS AND MAINTENANCE MANUAL

**Research Project Y-2811
Task 6**

**Washington State Highway Commission
Department of Highways
and In cooperation with
U.S. Department of Transportation
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SECTION I
GENERAL INFORMATION

1.1 Introduction

The time allotted for obtaining pavement condition ratings and to integrate these into a prioritized rehabilitation program for a given road system can be substantially reduced through improved data collection techniques. To gather, record, and process the field data more efficiently, it was necessary to develop a system that would speed up the field data collection process and eliminate the handwritten field coding and office hand entry of the data and allow direct input of the data into the main computer.

To accomplish this the University of Washington developed and built a prototype portable pavement rating device for evaluation by the Washington Department of Transportation. Correlation and operational tests of the prototype were conducted by WSDOT personnel to check operator usability and computer compatibility. These tests were performed by completing actual pavement condition surveys using the current method and the new method of survey. A high degree of correlation was found. The raters became proficient with the new technique of rating rather quickly. Computer compatibility was tested with the application of real data to the main computer and checking the usability of the data within the pavement management system computer programs.

1.2 Specification - Field Unit

See the individual manuals for each of the pieces of hardware in question for specific details. The specifications pertaining to the overall field system are as follows:

Operating Temperature: 40 F to 120 F

The unit less the printer has been successfully tested down to 28 degrees Fahrenheit. The manufacturers minimum temperature specification on the tape drive, however, is 40 F and efforts should be made to keep the unit at or above this temperature if possible while in use.

Storage Temperature: 0 F to 150 F

Tape Storage: Unformatted (450 foot tape)
17 Megabytes

Formatted
5 Megabytes
512 Bytes per Record
10500 (512 Byte) Records per Tape

Tape Format - Using 82 samples per 0.1 mile intervals
(Default Values) and 10 Sequences

4 Bytes per Sample of Keyboard
2 (512 Byte) Records per 0.1 mile Sequence
20 (512 Byte) Records per Mile
515 Miles Per Tape

Magnetic Tape Cartridges: 3M Scotch P/N DC 300XL or
DEI HI REL DATA P/N 301522-2

Power: 12Vdc @ 1.5 Amps w/o tape drive
3.5 Amps with tape drive

Vehicle Speed - Maximum Sampling Rate:

1.3 Supplies and Accessories

The only supplies required for the operation of the field pavement survey unit are the magnetic tape cartridges and the paper for the printer (See Appendices E through I). No other accessories are available or required for the field unit. However, the IBM PC/XT has almost an unlimited number of accessories and a larger hard disk drive maybe required to handle the large amounts of data that are to be collected. Either a single drive with one hundred plus megabytes or a dual 20 megabyte removable hard disk drive is recommended.

Two additional accessories, which are relatively inexpensive but are necessary for doing extensive data analysis are a BASIC complier and an 8087 math co-processor. These two items will increase the computers performance and will decrease the time required to read and analyze the data.

SECTION II INSTALLATION

2.1 General

The installation procedure involves the removal of the various components from within the carrying case and the connection of the various elements to the main microprocessor control unit. This includes the connection of the cables for the keyboard, remote transcrack unit, the hand terminal, the odometer connection and the 12 Volt DC power cable. Once all of these leads are connected and the power switch is turned on the control of the system is automatically taken over by the hand terminal. At this point the simple menu items displayed on the hand terminal will direct the operator through the setup and control of the system.

2.2 Power Requirements

The only power requirements for the use of the pavement survey unit is 12 Volts direct current at approximately 3.5 Amperes maximum. There is also an internal battery back up on part of the system RAM (internal Random Access Memory). This unit is good for approximately 10 years and retains the initial input variables and set parameters, along with pertinent information associated with the operation of the equipment. This means that the operator does not need to re-enter all of the setup information every time the system is turned on and off.

2.3 Front Panel Connections

There are four front panel connections associated with the setting up of the pavement survey unit. These are the 50 pin ribbon cable on the keyboard and the cables from the hand terminal, the remote transverse crack and odometer, and the main power cable. All connectors are polarized. It is impossible to plug a cable in wrong or into a wrong receptacle (See Figure 4).

2.4 Keyboard

All that is required for the installation of the keyboard is to plug the 50 pin connector attached to the unit into its receptacle on the lower lefthand corner of the pavement survey unit (See Figure 4).

2.5 Hand Terminal

The hand terminal is a full ASCII terminal with all the capabilities of a regular computer terminal except for the fact that it is limited to four sixteen character lines of display. It also has four programmable special function keys across the top of the unit. These keys are used extensively in the setup and control of the pavement survey unit.

The hand terminal is powered from the microprocessor control unit and must be plugged in to be operational. It will come on automatically when the microprocessor control unit is switched on.

2.6 Tape Cartridge Drive

The tape cartridge must be placed into the vertical slot on the righthand side of the microprocessor control unit with the metal side of the tape cartridge facing away from the connectors. The cartridge is aligned with the guiding framework and slid firmly and completely into the slot. It should only protrude about 3/4 of inch. The tape can be installed before the power is turned on and can be left in the instrument when it is closed up. Installing the cartridge before the unit is powered up will prevent the tape from being rewound when the power is turned on. This can save time and possible problems and is recommended while in regular use.

2.7 Printer

The only installation associated with the printer is the paper roll. The face of the printer slides out to give access. The factory instruction procedure should be followed, (See the manual, Appendix I).

2.8 Odometer

The odometer input used by the microprocessor control unit for distance and position calculations is connected into the system via the remote transverse crack connector. The coiled cable coming from the remote transverse crack connector joins into a male-female jumper connection which ties into the vehicles

distance measuring equipment without interfering with its normal operation. The cable stretches to give about six feet of distance between the microprocessor control unit and the vehicle's distance measuring equipment display.

Be sure that the power to the vehicle's distance measuring equipment is turned off before the jumper is installed or else the microprocessor control unit and/or the distance measuring equipment may be damaged. The jumper is wired for the Transwave distance measuring equipment (Model NK-1200, See Appendix E and Figure 16). If any other type of equipment is used check to see that the ground wire is connected to the shield and that the logic signal is TTL compatible and on pin 5. The manufacturer's manual provided with the unit used for the prototype development did not give the proper pin outs for this connector. Therefore, take caution and be sure that it is wired into the system properly. Any configuration changes on the other pins will not affect the operation of the system.

SECTION III
OPERATION

3.1 General

The operation of the field unit is controlled through the hand terminal and a series of menu items. The hand terminal is limited to four lines of sixteen characters each and thus leads to some nesting of the different menu lists and items (See Figure 1). However, the hand terminal is only required during initial set up procedures under most circumstances and thus lends itself well to this type of control.

Alphanumeric data can also be entered into the unit during or between runs. This is a little cumbersome with this type of terminal but is still practical. Any type of ASCII terminal or portable microcomputer unit could be adapted for use with the field unit if large amounts of alphanumeric data are required. Each interval (usually 0.1 miles) can contain up to 300 bytes (ASCII characters) of alphanumeric information in addition to the surface condition data. This is about 19 lines of text on the hand terminal.

The operation of the field pavement survey unit is as follows: The power is turned on once all leads have been installed (See section II). The control is automatically switched to the hand terminal and the initial menu is displayed on the LCD screen (See Figure 1 & Section 6.2). The set up data is entered and the system is initiated by pressing the START and ENTER keys

(See Section 3.8 below). The unit will begin collecting data when the vehicle reaches the BEGIN MILE or immediately if the BEGIN MILE and the ODOMETER are set to the same value. The BEGIN MILE, END MILE and the ODOMETER readings will be displayed continuously on the hand terminal once the system is initiated.

The system is connected directly to the vehicles odometer output, which is its primary control signal. Once the unit begins to collect data a red LED will flash on the face of the keyboard (See Figure 2). The unit will automatically sample all of the keys on the keyboard (except the five left most CONTROL KEYS) and store the status of each key on tape at the rate or spacing specified during the set up procedure (samples per interval, See Figure 1 & Section 6.2).

The data sequence is defined as the distance between the BEGIN and END MILE marks. The begin mile - end mile sequence is then divided into intervals, which are usually selected to be one tenth of a mile. Associated with each interval is a 300 byte alphanumeric data storage area on the tape. Up to the 300 bytes of data can be entered at the beginning of each sequence or at any one of the intervals within the sequence. To enter alphanumeric data at an interval break, the vehicle must be stopped and the PAUSE and ENTER keys must be pressed on the CONTROL KEYS section of the keyboard. A menu will appear instructing the operator to press F1 to enter the information. When completed, the menu will direct the operator to push the F2 key to begin normal operation again(See Figure 1).

The vehicle speed that can be obtained while still collecting valid data is dependent on the number of samples per interval and the initial length. Under default operations (82 samples per tenth mile interval) the maximum speed is approximately 50 mph.

The use of the printer at present requires that the vehicle come to a stop at the end of each interval to eliminate any or all data loss. The system still functions properly if not stopped. However, a number of samples will be lost at the beginning of each interval. Future modifications will eliminate this problem by putting a buffer on the printer.

3.2 Front Panel

The only controls associated with the front panel which are relevant for the operation of the field unit is the on-off switch, the printer controls, the installation of the magnetic tape cartridge and the power plug. Once the unit has been plugged into the cigarette lighter of the vehicle or attached directly to the battery using the clip leads that are provide with the unit, turn on the power switch and control will be automatically transferred to the hand terminal. This takes about 5 seconds while the system goes through some self checks. If the unit does not appear to function properly, the system can be reset by turning the power switch off and back on again. The data that has been entered will not be lost since the memory unit associated with the system set up is backed up by an internal battery and

will not have to be reentered. The clock will have to be reset if desired, however. If the problem persists, try resetting the non-volatile memory (See Figure 1 & Section 6.2).

3.3 Keyboard

The keyboard is the primary data entry device. It is also used to start and stop the system and to control some of the tape functions or operations. The keyboard is separated into seven different sections. The first is the CONTROL KEYS section. This section is used to start and stop the actual data collection, to manually place an extra end of file (EOF) on the tape, to control the pavement exempt function and for the selection of the pavement type.

Once the initializing or set up data associated with the hand terminal operation has been completed the unit will display a message that control has been transferred to the control rating panel (CRP) or keyboard and request that you press the START or STOP button (See Figure 1). Once these keys have been pressed the unit will begin sampling at the specified BEGIN MILE or immediately if the ODOMETER reading and the BEGIN MILE reading are the same. The unit will start at the END MILE and count in reverse if the sign in front of the interval variable is set to negative.

The PAV EXMT. (pavement exempt) key is used to exclude or stop automatic data entry by the system while still maintaining the proper mileage count. This function is used to eliminate

things like bridges or pavement sections that are not to be included in the final data.

The BST/ACP key is used to select the type of pavement that is being surveyed. This key can be changed while data is being automatically collected.

The second section of the keyboard is the SPECIAL FUNCTION KEYS. In general, these keys can be used for any function that the operator desires. The first two keys are push on - push off and will record data continuously while the LED (key) is on. The last three are momentary on (reset by the microprocessor unit), which means they will record a single value to the tape each time they are pushed. These keys are generally used for counting or for flagging significant points of interest. At present, the F1 key is being used in conjunction with the PATCHING section to indicate FULL DEPTH patching. This function was left out of the initial design specifications and will be added to future units just below the existing BST and ACP keys on the right side of the PATCHING section.

The normal use of the SPECIAL FUNCTION KEYS would be to specify, in the alphanumeric data entry mode, the desired function of each key. Then when the tape is read and analyzed the operator of the IBM PC/XT system can read this information and interpret the data accordingly.

The next five sections make up the main data entry portion of the keyboard. The exact use and function of these keys is defined in section 6.4. In general they function similar to the

categories on the original field survey forms used in previous manual pavement survey procedures. These keys are sampled automatically at the preset sampling interval and the operator simply presses the keys from the moving vehicle as he observes the different distress features in or on the roadway.

3.4 Hand Terminal

The hand terminal is powered directly from the microcomputer control unit and comes on with the main power switch. The unit is a standard ASCII computer terminal other than it is limited to four lines of sixteen characters each and that the keyboard is much smaller and has its own unique control procedures. See the reference manual in Appendix G for details on how to operate this unit. Its only function is to operate as a terminal and to allow the operator to enter the data to the microprocessor control unit which is required to control and operate the overall field pavement survey system.

3.5 Tape Cartridge Drive

Most functions of the tape cartridge drive are controlled automatically by the microprocessor control unit. The tape is manually inserted into the tape cartridge vertical slot on the righthand side of the field unit front panel (See Figure 3). If the power is on the tape will automatically rewind and position itself at the beginning of tape on track one. If the operator would like to start at the position he last stopped, the tape

should be left in the drive or replaced before the power is turned on.

Minimal tape control is supplied under the hand terminal control. This includes the option to define whether or not you are making a new run if a new run is selected the system will rewind the tape before you begin the the next sequence (See Figure 1). The system places a double EOF at the end of the tape automatically after each data sequence or at the end of the last successfully completed tape operation.

There can be more than one double EOF on a tape, therefore the operator may need to search the tape to determine the location of the last end of tape. If a problem should occur or if the operator would like to be able to find his location on the tape at a later time he can manually put a double EOF on the tape by pressing the EOF key followed by the ENTER key twice.

3.6 Printer

The printer is controlled through the hand terminal control menu and is either turned on or off (See figure 1). When off the printer plays no role in the operation of the field equipment. In the on status the printer will print a summary report at the end of each interval. This report lists the accumulated number of points associated with each of the CRP sections.

3.7 Odometer

The odometer signal is the only item that has to be supplied by the operator other than the 12Vdc power and the tape cartridges and printer paper. This signal must be TTL compatible and corresponds to the number of counts per mile in the set up menu list (See Figure 1 and Section 3.8). The unit can be calibrated to whatever input frequency that is provided.

To calibrate the unit follow the instructions in the menu (See Figure 1). Once in the calibrate mode the calibration process is initiated by pressing the START key followed by the ENTER key, at a known mile post. The calibration process is completed by pressing the STOP key followed by the ENTER key at a second known mile post. The system will ask for the distance traveled and from this will compute the odometer factor and store this in memory. Record this value manually when going through the input parameters. It will have to be reentered if and when the system is re-initialized.

3.8 Menu Driven Control System (See Figure 1)

When the system is first turned on, the Hand Terminal will go through a five second self test sequence to check out its own functions. At the same time the microprocesor control unit is running through a series of its own self tests. If everything is in working order, the hand terminal will display the MAIN MENU (See Figure 1 & Section 6.2). If the system does not display the

Main Menu after 10 seconds or a different menu shows, turn the power switch off and on and try again. If it still does not work, try resetting the non-volatile memory or refer to section 7.1.

The hand terminal has four special function keys F1, F2, F3, and F4. These keys are used to operate the menu control system. The acronym above each special function key or the menu itself defines the operation of that particular key for that particular menu operation, (see Figures 1 and 3).

MAIN MENU

This is the most basic menu item. It is the first menu to come on when power is applied and the final menu prior to starting the unit. The user is faced with three options:

- F1 System Setup
- F2 System Ready
- F3 System Init.

System Setup - F1

This is used to enter the initial set up data or to change, check, or calibrate the odometer before starting a sequence. Selection of this item will send the hand terminal to MENU 2. The vehicle must be stopped while entering all input variables.

System Ready - F2

This is used when the operator is satisfied with all the system parameters. After selecting this option, the hand terminal

will ask if this is going on a new tape. If so, the tape will be rewound before continuing on, otherwise the system will start with the tape at its present position. Whenever a tape is inserted into the unit with the power on, it is automatically rewound. Therefore, if the tape is not to be rewound insert the tape before switching on the power. After selecting the tape option the hand terminal will display:

Control By CRP
START to Begin
STOP to End

This is to remind the operator that the hand terminal is no longer in control and that the CRP is now waiting for the operator to react. If the operator wishes to return control to the hand terminal to change something before starting, pressing the STOP key followed by the ENTER key on the CRP. The MAIN MENU will appear and nothing will be written to the tape. Once START is pressed followed by the ENTER key, the hand terminal will display the BEGIN MILE, END MILE and the ODOMETER reading, which is updated continuously prior to sampling and once every interval there after. This updating is done following all other computer operations. Therefore, the value displayed on the terminal will be somewhat greater than the actual 0.1 mile interval value. The system will begin sampling as defined by the control variables.

System Initiate

This is used to reinitialize the system. It is a good

practice to use this function from time to time, especial when first turning the system on. Since the system is designed to retain the previous information and system parameters after the power is turned off, the memory will tend to collect unnecessary values which could affect the operation of the system. A good example of this would be if the last user pulled out the tape while it was running, crashing the system. Reinitializing the system will reset the computers memory, reload all the default values, change parameters for the actual values, and then reset the system's hardware and connections.

MENU 2 (F1 in MAIN MENU 1)

This menu gives the operator the choice of whether to look at or reset the parameters, calibrate the odometer, or exit back to the main menu. After selecting this option the terminal will display:

```
F1 Parameter
F2 Odometer CAL
```

Parameter - F1

This option is used if the operator wishes to change or look at any parameters, or enter any comments into the comment buffer. The selection of this option will send the hand terminal to MENU 3.

Odometer CAL - F2

This option is used to calibrate the odometer. See section

5.2 for the use of this option. Any exits from within the calibration section will always return to Menu 2.

MENU 3 (F1 in MENU 2)

In this menu the operator has the choice of working with the system parameters or using the comment section. Pressing the Exit (F4) will return the hand terminal back to the Main Menu. The terminal will display the following:

```
F1 Change Param
F2 Update Param
F3 Comments
```

Change Param - F1

This option is used to display and/or change any of the system parameters or sequence information which will be written on the tape and control the system. There are three classes of parameters; A) Those parameters which must have a value for the system to run a sequence and are loaded with a default value when the system is initialized, B) Those parameters which are not needed for a successful run of a sequence but are still loaded with a default value when the system is initialized, and C) Those parameters which are used only for information that is written on the sequence header and interval summaries. They will not affect the operation of the system and are set to question marks when the system is initialized.

There are 14 parameters which the operator may page through by pressing either the PRV (F1) or the NXT (F2) keys. The items wrap around so that pressing NXT at the end of the parameters

will take the operator back to the beginning, and pressing PRV at the beginning will take the operator to the end of the parameters. Pressing EXT (F4) at any time will return the operator back to Menu 3 and any changes that were made will be entered into the computers memory. The following is a list of the menu items;

Parameter	Class	Default Value
SYSTEM CODE/RECORD No.	Class C	Default ?????

This is arbitrary and can be used at the operators discretion for tape and/or sequence identification.

TEAM ID	Class C	Default ??.??
---------	---------	---------------

Used for the initials of a two man team. Example, John Doe and Harvey Smith would be entered as JD.HS .

DATE	Class B	Default 01/01/85
------	---------	------------------

The date is stored in memory when power is turned off, however, it is not updated. To enter the date simply enter the desired numbers from the hand terminal's keyboard. Follow the instructions above the function keys or use the backspace key on the terminal to edit the input.

CURRENT TIME - 24 hour clock	Class B	Default 00:00:00
------------------------------	---------	------------------

In this menu item is a SET (F3) function which is used to

set the time. After power is removed the time is lost and will return as a random time if the system is not first initialized. To enter the time simply enter the desired numbers from the hand terminal's keyboard. Follow the instructions above the function keys or use the backspace key on the terminal to edit the input. Press the function key below SET on the terminal to enter the time.

DISTRICT-STATE ROUTE-CLASS Class C Default ?.???.?

CONTROL SECTION/SEQUENCE Class C Default ?????.???

The use of these input variables is self explanatory and relate to WSDOT's highway classification and labeling system.

LANE Class C Default ?

Used for indicating which lane is being checked. To indicate both lanes, enter a "1". Use a "2" for the left lane and a "3" for the right.

ODOMETER FACTOR Class A Default 4100

This number represents the number of positive pulse transitions given by the distance measuring equipment sensor in one mile. This number may vary slightly from vehicle to vehicle or from factors such as tire wear. Use the odometer calibration to find the exact value for the vehicle which is to be used (See Section 3.7 and 6.7). The odometer factor can be entered manually or computed and stored automatically using the odometer calibration procedure. Once a calibration has been run, the

number that is obtained should be recorded so that it can be entered by hand if and when the non-volatile memory is reset (Initialized). The default value is close to the actual number.

ODOMETER READING Class A Default 000.0000

This reading is used to reference the vehicle from the Begin and End mile locations. Usually this would be equal to a mile post number where the vehicle is sitting when the system is setup.

BEGIN MILE Class A Default 000.0000

The defined point where the system will start sampling the data keys and write the data on tape.

END MILE Class A Default 001.0000

The defined point where the system will stop collecting data, write what data it has collected to tape, and return control to the hand terminal with the MAIN MENU.

INTERVAL DIRECTION/LENGTH Class A Default +0.1000

This is the length of the individual intervals. The number is preceded by a "+" or "-" sign to indicate whether the system is to go from the BEGIN MILE to the END MILE or reverse (to increment or decrement the mile counter). An example of decrementing would be if the vehicle turned around and went the

opposite direction for another sequence for the other side of the road.

NUMBER of SAMPLES per INTERVAL Class A Default 82

This determines how many times per interval the system will sample the CRP for data. This number must be an even multiple of the odometer factor, and if it isn't, the system will recompute the numbers entered and automatically select the closed even set of values.

The algorithm used for computing the actual number of samples per interval from the values entered is as follows:

Let

ODFACT = Odometer factor (Number of signal pulses per mile produced by the odometer)

NSAMP = Number of samples per interval requested

INTLEN = Interval length requested

Then, the factor

$$\text{COUNFAC} = (\text{ODFACT})(\text{INTLEN}) / (\text{NSAMP})$$

rounded to the nearest integer gives the number of pulses between any two scans (or samples). Because of this "rounding off", NSAMP will have to be adjusted as follows;

NSAMP ----> NSAMP' = (ODFACT)(INTLEN) / (COUNFAC) rounded off to the nearest integer. Rounding off of NSAMP' will result in a new interval length given by,

INTLEN ----> INTLEN' = (NSAMP')(COUNFAC) / (ODFACT)

PRINTER ON/OFF Class B Default OFF

This controls the option to have a report of sample accumulations printed out at the end of each interval. At present, if this option is selected, the operator will have to drive much slower towards the end of each interval to avoid loosing data on the beginning of the next interval. A print buffer is to be added to the system which will eliminate this problem.

3.9 IBM PC/XT Computer System

The IBM PC/XT computer system is an integral part of the overall pavement survey system. It is used to read, edit and display the data from the tapes that are recorded in the field. It also has the software required to do the initial data averaging and file development required to get the data into the interpreting program in their overall pavement management system.

This system consists of an IBM PC/XT with a printer and a Digi-Data Corporation model 6450 cartridge tape drive. Also, software has been developed to control the tape drive, to read, edit and analyze the data and to put the data in a form that can be entered directly pavement management system.

Users Guide For Pavement Survey Unit Software

TDRIV is a program designed to read data tapes from the field pavement survey unit. In addition to displaying the sequence and interval summaries, TDRIV can display individual samples or compute severity, extent and deduct values for the different intervals.

Starting TDRIV

TDRIV is located on the hard disk in directory \DOT, so to make running and loading easier, it is a good idea to move into this directory before running the program. To change into \DOT, type

```
cd \dot <cr>
```

If, however, you want the files you create while running TDRIV to end up in a directory other than \DOT then you should go to that directory instead and use a different form of the load command discussed below.

Since TDRIV is (presently) written in interpreted BASIC, the first step in running it is to load the BASIC interpreter. This is done with the statement:

```
basic /c:l000 /s:l000 <cr>
```

where <cr> indicates a carriage return. You should now see a welcome message from BASIC. Next type

```
load "tdriv.bas" <cr>
```

from within the directory \DOT or

```
load "c:\dot\tdriv.bas" <cr>
```

from any other directory. You should see an "Ok," prompt when this is completed.

To actually start the program, simply type

```
run <cr>
```

TDRIV's opening menu should now appear.

When you are done running TDRIV and are back at the BASIC command level (the "Ok," prompt) type

```
system <cr>
```

to return to PC-DOS.

Running TDRIV

All of the functions in TDRIV are accessed from a main menu, (the one that comes up when the program is first started). The following sections will cover each option in detail.

1) Set Track

The cartridge tapes are formatted such that there are four logical tracks per tape. The set track function changes the track that the tape drive looks at and hence provides an easy way to skip a quarter of the tape at a time. One word of warning though, the tracks are arranged on the tape in a serpentine fashion so that the end of track one is at the beginning of track

two, etc. This means that if you are at the beginning of track one and switch to track two, you will be at the very end of track two and doing any sort of read operation will push you over onto track three. See Section 3.5,6.5 and Appendix H.

2) Rewind Tape

This will move to the beginning of track one and read the first sequence header, positioning you at sequence one, interval one.

3) Search for Summary

This will search through the tape sequentially from the current position looking for either the next interval summary record or a specific summary, if you gave it an interval number (See Section 6.5). This is a handy way to move long distances forward in a sequence.

One current problem involves trying to search past a tape error. The drive's search routine will return an error code and leave the tape positioned before the error, so that resubmitting the search will only reveal the same error. As of now, no simple way has been found to gain access to data in a sequence that was recorded with a tape error. The data in the following sequences is still good and accessible.

4) Read Current Header

This will read the current sequence header. If the tape is currently positioned in the first sequence then this command

behaves exactly like (2) and rewind the tape. Its main use occurs when the tape is positioned on some sequence other than the first. It can then be used either to recover from a "tape position lost" error without losing track of what sequence it was on or as a fast way to back up. As an example, if the current position was sequence 5, interval 40 (S5I40) and you wanted to move to interval 20 in the same sequence (S5I20) the fastest way to do it would be to read the current header (4) and then search for summary number 20 (3).

5) Dump Interval to Disk

This will dump all the data for a single interval to a disk file of the users choice, one sample per line.

6) Display Individual Samples

This option allows you to see which keys were depressed for each sample during an interval. The samples are displayed 20 at a time, with blanks representing no data, question marks representing invalid or default data and various mnemonic symbols (such as Sp for spalling, etc., See Appendix A and Section 6.5) representing valid data. After each screen of data you may enter either a carriage return to see the next 20 samples, a specific sample number to see 20 samples starting with that number, or a minus one (-1) to return to the main menu. You will be returned to the main menu automatically when all samples in an interval have been displayed.

7) Space Forward Interval

8) Reverse Space Interval

The forward/reverse space interval function will reposition the tape to the end of the following/preceding interval and then display the interval summary. Should the end/beginning of a sequence be encountered, the sequence header will be read and displayed.

9) Compute Summary Statistics

This will compute the severity, extent and deduct values for the current interval, and then display them to the screen following the interval summary. This operation entails a large amount of data manipulation and number crunching. The speed of these operations can be increased substantially by the use of a BASIC compiler and an 8087 math co-processor. Also, the amount of data being collected may become a consideration. An IBM PC/AT would also greatly improve performance. There are also co-processor type boards for the XT which can greatly improve its performance for a relatively low cost.

A new option is also available but the software modification have yet to be added. That is, at present the field system computes and stores the accumulated data associated with the severity, extent and deduct calculations. This mode will use these values directly and will be added to the IBM software by late spring and will substantially enhance the overall performance of this system.

10) Forward Space Sequence (file)

11) Reverse Space Sequence

The forward/reverse space sequence function moves to the beginning of the following/preceding sequence and reads and displays the sequence header.

12) Retension Tape

Spins the tape cartridge from one end to the other to even out the tape tension. This can sometimes cure intermittent tape errors, if the tape has been sitting for a while or has undergone a great deal of stop and start motion.

13) Autosummary of Current Sequence

This function computes severities, extents and deduct values for all intervals in the current sequence and writes the data into two files. The two files are referred to as the header and the data files.

<type><state_route><dir><beg_mile>.DAT

where <type> is either H or D for header and data files respectively, <state_route> is the state route number, <dir> is the direction of travel (either P or M for increasing or decreasing mile number) and <beg_mile> is the beginning milepost number. These two files are the two required for input to the dBase programs for later manipulation.

14) Stop

Stops the program and returns you to the basic command level.

Common Errors and Problems

Probably the most common error is caused by the tape drive not being properly set or reset. If the tape drive has not been used since it has been turned on (the SELECT light is off), TDRIV will probably halt with an "I/O error in 550" message. The cause of this error has not been determined, but its occurrence causes the SELECT light to go on and hence prevents this problems repetition. Just type run again to restart the program and all should work well.

Another common problem is the program "hanging" and not returning to the menu on the first function selected. This is most likely caused by the tape drive being turned off or a connector having fallen off. Press CTRL and BREAK at the same time to halt the program, then check the switches and connectors before trying again.

Another error manifests itself with an "Illegal function call in 35" message. This probably means that you forgot the "/c:1000 /s:1000" parameters on the BASIC invocation.

dBASE program documentation

To load data files into dBase for the very first time, from within dBase type (you must have the dBASE III dot prompt on the screen).

SECTION IV

MAINTENANCE

4.1 General

The maintenance of the field equipment is limited to the tape drive, the keyboard and the printer. The other items are relatively maintenance free as long as everything is kept clean and dry. Consult the individual manufacturers manuals for the maintenance of the various items in the IBM PC/XT system.

4.2 Microcomputer Unit

This unit should not be removed or tampered with by other than a qualified electronics technician. There is no real maintenance required other than keeping the connectors clean and replaced if required. There is a fuses on the front panel that should be checked and replaced if the unit fails to come on when power is applied to the unit.

4.3 Keyboard

This unit should be kept clean and dry. It would be a good practice to periodically disassemble the unit and remove the three PCB cards and front cover and clean the unit with a freon spray and/or compressed air. By removing the six socket head cap screws on the cable end of the unit the complete assembly can be removed and disassembled. The individual keys are soldered to the top board and can be easily replaced if needed.

4.4 Hand Terminal

The hand terminal is environmentally sealed and should not require maintenance. However, the manufacturers manual should be studied carefully before using the unit.

4.5 Tape Cartridge Drive

The tape heads and surrounding area should be cleaned periodically using a series of clean cotton or foam swabs and alcohol. It is also generally recommended that the metal surfaces and the tape head be demagnetized a regular intervals, please consult the manual and/or the factory before doing this operation.

4.6 Printer

The paper will have to be replaced as needed, please consult the manual, see appendix I. The front panel pulls out to give access to the paper spindle. Cleaning of this area periodically is also recommended.

4.7 IBM PC/XT Computer System

Consult the applicable manufacturers literature for the maintenance of this equipment.

SECTION V

CALIBRATION

5.1 General

The only calibration associated with the overall system is in the field pavement survey unit. This calibration is used to determine the exact number of counts per mile that are given out by the odometer unit. This unit is mounted on the vehicle and is connected directly to the microprocessor control unit through the front panel (See Figure 4).

5.2 Odometer Calibration

The calibration of the odometer requires having a stretch of road with known mile post marks. The operator selects the odometer calibration option from the hand terminal (See MENU 2, & Figure 1), the hand terminal will then remind the operator to press the START key (followed by the ENTER key) when the vehicle is at the beginning mile post. When the vehicle comes to the end of the section or final mile post the operator presses the STOP key (again followed by ENTER). The pressing of the ENTER initiates the action, therefore, the START or STOP key can be pushed in advance and the ENTER key used to mark or start the action. The hand terminal will then ask for the distance travelled to the nearest tenth of a mile. Once entered the hand terminal will return the operator to Menu 2 and the system will automatically log the new value for the Odometer Factor into the parameter section of it's memory.

SECTION VI
THEORY OF OPERATION

6.1 General

The pavement condition recording and computing device is a microprocessor-controlled, data acquisition and reduction system which uses a combination of manual inputs and an odometer readings to develop pavement condition reports. These reports are printed on the system printer and written to a standard magnetic tape cartridge along with the raw data for later inclusion in the Washington State Department of Transportation (WSDOT) pavement management data base (WSPMS).

The device, including all of its attendant equipment, is fully portable and can be used in any motor vehicle that has an odometer pulse generator (preferably producing approximately 4,000 TTL level counts per mile) and 12 Vdc power source.

6.2 Microcomputer Control Unit

This is the main component and consists of a microprocessor-based control unit with power supply, input digital signal capability and input/output communication ports. A control rating panel (CRP), a hand terminal, remote transcrack unit, a tape drive and a printer are all connected to this unit. This complete system is housed in a portable moisture resistant case.

6.3 Control Rating Panel - Keyboard

The rating portion of the CRP regulates the monitoring of the pavement defect data. The CRP maintains a running evaluation of the pavement condition. The microprocessor control unit then samples (scans) these inputs at a fixed distance interval (approximately 4,000 scans per mile or any even integer division thereof). It records this raw information on magnetic tape along with the data accumulations for each input variable and any desired alphanumeric text. The terminal also displays the BEGIN MILE, END MILE and the ODOMETER READING, while data is being collected.

Control Keys

The starting sequence will allow the automatic initiation of a test run. The odometer must be set to a known milepost prior to the start of the test run. When the odometer is incremented or decremented to the starting mile value, data collection automatically begins. The BEGIN MILE is always numerically less than the END MILE. In the decrementing direction, the value keyed in as END MILE will start the data collection. Auto start cannot be modified while collecting data, but it can be deactivated by pressing the STOP plus the ENTER key on the CRP.

A plus or minus sign in front of the interval value will select whether the odometer will increment or decrement. When in the decrement mode, the END MILE value is considered the start of the measuring sequence and the BEGIN MILE the finish.

The BST/ACP key (push on-push off) records the pavement type as ACP when not activated (light off) and BST when activated (light on).

The STOP key followed by the ENTER key (momentary contact) will halt data collection, terminate the run, and print out and record the accumulated data.

The PAV'T EXEMPT key (push-on-push-off) halts data collection while activated (light on) and resume data collection when deactivated (light off). The odometer continues working through this phase and results in a normal run with fewer samples for that particular interval. This is used to exclude unwanted roadway sections such as bridge decks. The PAV EXMT and the BST/ACP keys are both turned off by either pressing the key again or when the computer resets the CRP at start up.

The END OF FILE key places an end of file (EOF) mark on the tape each time this key and the ENTER key is pushed. This is used for tape control. If problems occur a double EOF on the tape will allow the repositioning of the tape back to this position.

The PAUSE key will return the menu control back to the operator and allow for parameter modification, updating, report generation, addition of comments to that tape interval and system restart.

The STOP, PAUSE, and START keys are tied together so that only one of these keys will be on at a time. The only way to turn off any one of these keys is to press one of the others or

when the computer resets the CRP. When any of these keys are pressed the ENTER key will light up to remind the operator to press ENTER. This must be done before the actual function is performed by the microprocessor unit.

The EOF (End of File) key is a push-on-push-off key which will also light the ENTER key. The ENTER key is to get the computers attention so that if the EOF, STOP, PAUSE, or START keys were pressed by accident, the operator could change the situation before the computer reacted. If the EOF was pressed by accident, pressing it again will turn it off, the ENTER key will stay on but pressing it will only turn the light off. After the computer has recognized the ENTER key and the key which turned it on, the computer will toggle the Ent. STRB line which will turn off the ENTER key light and the EOF if it was pressed. The computer will not turn the STOP, PAUSE, or START lights off, however, so that the operator will know which mode the system is in at all times. The PAV EXMT. and the BST/ACP keys will not affect the ENTER key.

Special Function Keys

The special function keys are user definable keys and can be used for anything the operator wishes. To use these keys the operator simply defines what they are to be used for in the comment section and proceeds as defined. The first two keys (F1 & F2) are push on - push off keys, that is, their status is recorded to tape continuously whether on or off. The last three (F3, F4, & F5) are momentary-on keys and are used for counting

items such as pot holes or for flagging purposes.

The F3, F4, and F5 keys will stay on until the computer reads them, after which the computer will toggle the M STRB line which will turn them off. This assures the operator that the data has been read. If the vehicle stops in the middle of a sequence and one of these three keys are pressed, they will stay on until the vehicle moves forward enough for the system to take another sample of the keyboard. When the vehicle is moving at a reasonable speed, this interaction between the keys and the computer will be such that the keys will appear to be a momentary switches. The transcrack keys also function in this same way.

Control Rating Keys

The rating portion of the CRP is divided into five distinct, visually-separated, rating categories. The categories are laid out from left to right as follows: Alligator cracking, longitudinal cracking, transverse cracking, patching, and raveling or flushing.

The four "CLR" buttons are used to clear or deactivate any defect keys that are in the active status, but will not erase any of the accumulated data in the memory registers. All keys have LED lights in them to indicate active status ("on"). The CLR key will light if an invalid selection has been made in that category.

A hand held rating device is included for the counting of transverse cracks by the driver. The device is identical to the "TRANS CRACK" section on the keyboard and is connected to the main panel through a front panel connector and a six foot long expandable cord.

The CRP is scanned and data stored to tape and accumulated in memory at up to the odometer factor rate per mile. This depends on the input variables, samples per interval and interval length. The BEGIN MILE - END MILE sequence is separated into intervals of any desired length.

The keyboard (CRP) contains three printed circuit boards (PCB's), a housing and a front panel with keys (See Figures 2, 6 - 9 & 12 - 15). The top PCB supports only the switches (keys) and the LEDs (Light Emitting Diodes) for the individual keys. The second board consists of two parts. The main part is the circuitry which handles the switch debounce for the data switches and the LED drivers. The second part is the circuitry for the control switches, This includes the logic circuitry for these switches. The third board consists of the logic circuitry for the data switches and the buffers for the signals going to and coming from the microprocessor control unit.

Each key has its own set of logic circuitry consisting of a flip-flop and a delay buffer (See Figures 15 and 16). Through jumpers on the board the switch can be made to function as a momentary push-on, a momentary push-on with computer reset, or a push-on-push-off type switch. Each switch can be set or reset by the computer (all keys at once) and can be cleared by any

selected clear key or the pressing of another data key in the respective category.

Control Rating Panel Defect Categories

The ALLIGATOR CRACKING and the LONGITUDINAL CRACKING categories each have five keys. At least one key must be activated in either category to indicate a defect. Two keys can be activated at the same time under alligator or longitudinal cracking to indicate defects in each wheel path. Under longitudinal cracking, any combination of these two keys can occur because of multiple cracks. If the "+1" key is pushed, it will duplicate the greatest severity that is active in that category. Activating the "+1" key under alligator cracking indicates two simultaneous defects at the same severity as the key activated in the left hand column. Each time the computer scans the panel, it records the active condition shown on the panel; one count per activity. If the "+1" is active, then the most severe condition indicated gets two counts.

All these keys are push-on-push-off keys (except for the CLR keys). When the CLR key is pressed, all the keys in its category will turn off. If the +1 is pressed by itself or if the HL, >1/4, and the SP are all on at the same time, the CLR key will light up to indicate that this is an invalid situation. Pressing the unwanted key again or the CLR key will remedy the situation.

The severity (S), extent (E) and deduct value (D) are

calculated as follows:

Alligator Cracking Formulas

$$S_{AC} = \frac{C_1 + 2C_2 + 3C_3}{C_1 + C_2 + C_3} \quad (\text{Round to nearest 10th})$$

$$E_{AC} = \frac{2(C_1 + C_2 + C_3) + 1}{N_s} \quad (\text{rounded to nearest 10th after checking E for limits})$$

$$\begin{aligned} D_{AC} &= 15(S_{AC}-1) + 10(E_{AC}-1) + 10 \quad (\text{Deduct}) \\ &= 5(3S_{AC} + 2E_{AC}-3) \end{aligned}$$

C_1 = counts of "HL" (hairline) severity in each wheel path

C_2 = counts of ">1/4" (over 1/4") severity in each wheel path

C_3 = counts of "SP" (spalling) severity in each wheel path

N_s = Number of times panel scanned in rated length

If $C_1 + C_2 + C_3 = 0$, then print "(0.0, 0.0)"

If $E < 1.03$, then print "(0.0, 0.0)"

If $E > 4.0$, then $E = 4.0$

Longitudinal Cracking

$$S_{LC} = \frac{C_1 + 2C_2 + 3C_3}{C_1 + C_2 + C_3} \quad (\text{Round to nearest 10th})$$

$$E_{LC} = \frac{C_1 + C_2 + C_3 + 1}{N_s} \quad (\text{round to nearest 10th after checking } E < 1.10)$$

$$D_{Lc} = 10[(S_{Lc}-1)+(E_{Lc}-1)] + 5$$

$$= 10(S_{Lc} + E_{Lc}) - 15$$

C₁ = Counts of "HL" severity along 1 or more cracks

C₂ = Counts of ">1/4" severity along 1 or more cracks

C₃ = Counts of "SP" severity along 1 or more cracks

N_s = Number of times panel scanned in rated length

If C₁ + C₂ + C₃ = 0, then print "(0.0, 0.0)"

If E < 1.01, then print "(0.0, 0.0)"

Each crack is counted separately.

The TRANSVERSE CRACKING category has three keys. Each push of a key will count one in the computer at that particular severity. The computer will only scan this category for severity and the data is sent directly to the computer as it is counted.

All these keys are push-on-stay-on keys with computer reset. They are tied together so that only one can be on at a time and it will stay on until the computer reads it and shuts it off. They are, therefore, used to count individual cracks.

The severity (S_{TC}), extent (E_{TC}) and deduct value (D) are calculated as follows:

$$S_{TC} = \frac{N_1 + 2N_2 + 3N_3}{N_1 + N_2 + N_3} \quad (\text{round to nearest 10th})$$

$$E_{TC} = 0.78 + \frac{22N}{L} \quad (\text{round to nearest 10th after checking for } E < 1.00)$$

$$D_{TC} = 5[(S_{TC}-1) + (E_{TC}-1) + 1] \quad (\text{Deduct})$$

$$= 5(S_{TC} + E_{TC} - 1)$$

$$N = N_1 + N_2 + N_3$$

N_1 = Number of "HL" cracks

N_2 = Number of ">1/4" cracks

N_3 = Number of "SP" cracks

If $E > 3.0$, then make $E = 3.0$

If $E < 1.00$, then print "(0.0, 0.0)"

L = length of section in feet.

The PATCHING category has seven keys. The left column is used to measure extent when combined with distance and the right column is for severity. In each column, not more than one key can be active at one time. If another key is pushed when one is already active, the new one will then become active and cancel the other.

At present the F1 key is being used to indicate full depth patching and operates independently from the other keys in this category (This will be changed in future units). If a key is pressed in one column but not pressed in the other, the CLR key will light up to indicate that this is an invalid situation. Pressing a key in the other column or the CLR key will remedy this situation.

The severity (S_{PA}), extent (E_{PA}) and deduct value (D) are calculated as follows:

$$S_{PA} = \frac{B + 2A + 3A'}{B + A + A'} \quad (\text{round to nearest 10th})$$

$$E_{PA} = 0.92 + \frac{2.08 (B + A)}{N_s} \quad (\text{round to nearest 10th after checking for } E < 1.00)$$

$$D_{PA} = 10[(S_{PA}-1) + (E_{PA}-1) + 1] \quad (\text{deduct})$$

$$= 10(S_{PA} + E_{PA} - 1)$$

$$B = C_{B1/4} + 2C_{B1/2} + 3C_{B3/4} + 4C_{BF}$$

$$A = C_{A1/4} + 2C_{A1/2} + 3C_{A3/4} + 4C_{AF}$$

$$A' = C_{A'1/4} + 2C_{A'1/2} + 3C_{A'3/4} + 4C_{A'F}$$

$C_{B1/4}$ = Counts for 1/4 lal/4 lane BST patching

C_x = counts if activated button when scanned N_s times

N_s = Numbers of times scanned in

B = BST, A = ACP, A' = ACP(full depth), F = Full width

y = portion of lane width

C = Accumulated counts

If $E > 3.0$, then make $E = 3.0$

If $E < 1.00$, then print "(0.0, 0.0)"

If $B+A = 0$, then print "(0.0, 0.0)"

The RAVELING or FLUSHING category has nine keys. The left column defines the defect, the middle the severity, and the right

the extent. In each column, not more than one key can be active at any one time. If another key is pushed when one is already active, the new one will then become active and cancel the other. If there is a key pressed in one or two columns but not all three, the CLR key will light to show that this is an invalid condition. Pressing a key in each column or pressing the CLR key will remedy this situation.

The severity (S), and extent (E) are calculated as follows:

$$S_{RA} = \frac{SR_1 + 2SR_2 + 3SR_3}{N_s} \quad (\text{round to nearest 10th})$$

$$S_{FL} = \frac{SF_1 + 2SF_2 + 3SF_3}{N_s}$$

$$E_{RA} = \frac{ER_1 + 2ER_2 + 3ER_3}{N_s} \quad (\text{round to nearest 10th})$$

$$E_{FL} = \frac{EF_1 + 2EF_2 + 3EF_3}{N_s}$$

SF₁ = SR₁ = Accumulated counts at "slight" severity

SF₂ = SR₂ = Accumulated counts at "moderate" severity

SF₃ = SR₃ = Accumulated counts at severe" severity

N_s = Number of times scanned in rated length

EF₁ = ER₁ = Accumulated counts at "localized" extent

EF₂ = ER₂ = Accumulated counts at "wheel path" extent

EF₃ = ER₃ = Accumulated counts at "entire lane" extent

6.4 Hand Terminal

The hand terminal is a full ASCII terminal (regular computer terminal) except it is limited to four lines of sixteen characters each. It also has four programmable special function keys, which are used extensively for program control. The acronym above each key or the F1, F2, F3, or F4 specification in the menu text defines there individual functions.

Menu Variables

The control portion of the system allows input of project data as well as controlling the sequencing of a test. This control function is performed by using the hand held terminal with menu driven data input and the control key functions on the CRP.

The following is a description of the individual variables that are entered from the hand terminal (See Figure 1).

1. SYSTEM CD/REC:

This is a user definable input and is meant for sequence identification purposes.

2. TEAM INITIALS:

Two sets of two alpha-values are provided for entering two raters initials.

3. DATE: Month-day-year (00-00-00).

4. CURRENT TIME: - 24 Hour clock
5. DISTRICT/SIGN ROUTE/FUNCTIONAL CLASS:
District = one digit, sign route = up to three digits,
functional class = one digit (0-000-0).
6. CONTROL SECTION/CONTROL SECTION SEQUENCE:
Control section = four digits, control section sequence =
three digits (0000- 000).
7. LANE: Both = 1, right = 2, left = 3 (0).
8. ODOMETER FACTOR:
This is the number of counts per mile generated by the
odometer.
9. ODOMETER READING:
The current odometer reading is displayed on the hand
terminal while data is being collected and is entered
manually.
10. BEGIN MILE:
Normal operation will trigger data collection at this preset
mileage if the direction is incrementing; data collection
will end at this mileage if the direction is decrementing.
11. END MILE:
Data collection will automatically end at this preset
mileage and record the data to tape. If the printer option
is active a report is generated. Normal operation will

trigger data collection at this preset mileage if the direction is decrementing. A sequence is defined as the distance between the BEGIN MILE and the END MILE.

12. INTERVAL:

A preset distance interval at which the system will automatically terminate the relative accumulations and record this information to tape. If the print option is on a summary report is generated. Also a plus or minus sign in front of this variable controls whether the counting is incremented or decremented.

13. SAMPLES/INTERVAL:

This defines the resolution between samples.

14. PRINTER ON/OFF:

Activates or deactivates the printer option.

All of the above items are held in the memory after entry. The memory items are held until erased or modified. This part of the memory is non-volatile and will not be altered by unplugging or turning the unit off and on.

6.5 Tape Cartridge Drive

Most of cartridge tape control is handled automatically by the system software. The tape cartridge is rewound upon insertion (if the power is on) and positioned at the beginning of tape and on track one or it can be allowed to continue from the current tape position (the operator must be aware of which track he is on and set the system to the proper track if necessary). Also the

tape can be positioned at a double end of file mark which is automatically placed at the end of a tape if and when a data collection sequence has been completed or the system has been shut down. Also, the operator can place a double end of file on the tape using the keyboard. This is used for limited tape control. This will also allow for more efficient use of individual tapes. A software tape reset feature is provided to reinitialize a new tape when first starting a sequence of measurements. The filling of a tape with data or the removal of a tape sounds an audible alarm and initiates a menu sequence on the hand terminal. This allows for efficient tape management and control.

The tape drive is used for storing both the raw data and information which is important for keeping track of the data. When the system is first turned on the computer will set up the tape controller board (See Figure 5) for proper parity and bit count. Then the system will check the tape drive for its present status to verify that proper communications have been set up. If a status byte is not received the system will send the message "PLEASE TOGGLE THE POWER" to the hand terminal. After the parameters have been entered and the tape has been positioned to where the operator wishes, and the START button has been pushed, the system will write a 512 byte record at the beginning of the tape called the Sequence Header. This information is used to identify one sequence from another and is in the following

format:

STARTING	NO.of	
BYTE #	BYTES	DESCRIPTION
0	8	ASCII word "HEADER ". Used for locating

		the Sequence Header when reading the tape.
8	2	Zeros
10	1	The calculated number of records needed for one interval.
11	5	Zeros
16	4	ASCII System Code and Record
20	4	ASCII Team Letters
24	6	ASCII Date (Month/Day/Year)
30	6	ASCII Time (Hours/Minutes/Seconds)
36	1	ASCII District
37	3	ASCII State Route
40	1	ASCII Functional Class
41	4	ASCII Control Section
45	3	ASCII Control sequence
48	1	ASCII Lane
49	4	Odometer Reading *
53	5	Length of interval, the first byte is going to be either an ASCII "+" or "-". *
58	4	Odometer Factor *
62	4	Begin Mile *
66	4	End Mile *
70	40	Zeros
110	2	Number of samples per interval
112	4	Zeros
116	8	ASCII word "COMMENT "
124	300	Comment Buffer
424	88	Accumulations

* A hexadecimal number represented as hh.hh . Where hh is a two byte hex number representing either the integer number or the decimal number in 10 thousandths. Ex 10.20 would represent the decimal number 256.512 .

As the system collects data it writes it to the tape drive in 512 byte records. At the end of every interval (defined by the operator) the system will fill the remaining part of the current record with zeros. If there are less records than the calculated number of records per interval, the system will write blank records to the tape until there are enough records. This condition would result from extensive use of the pavement exempt key.

The system is now ready to write the Interval Summary record. The format is very similar to the Sequence Header and is as follows:

STARTING BYTE #	NO.of BYTES	DESCRIPTION
0	8	ASCII word "SUMMARY ".

8	2	Interval Sequence Number
10	1	The calculated number of records needed for one interval.
11	5	Zeros
16	4	ASCII System Code and Record
20	4	ASCII Team Letters
24	6	ASCII Date (Month/Day/Year)
30	6	ASCII Time (Hours/Minutes/Seconds)
36	1	ASCII District
37	3	ASCII State Route
40	1	ASCII Functional Class
41	4	ASCII Control Section
45	3	ASCII Control Sequence
48	1	ASCII Lane
49	4	Odometer Reading *
53	5	Length of interval, the first byte is going to be either an ASCII "+" or "-". *
58	4	Odometer Factor *
62	4	Begin Mile *
66	4	End Mile *
70	2	Alligator Crack Severity **
72	2	Alligator Crack Extent **
74	2	Longitudinal Crack Severity **
76	2	Longitudinal Crack Extent **
78	4	Zeros
82	2	Patching Severity **
84	2	Patching Extent **
86	2	Ravelling Severity **
88	2	Ravelling Extent **
90	2	Flushing Severity **
92	2	Flushing Extent **
94	2	Flag Button #1
96	2	Flag Button #2
98	2	Flag Button #3
100	2	Flag Button #4
102	2	Flag Button #5
104	2	Transverse Crack HL
106	2	Transverse Crack >1/4
108	2	Transverse Crack SP
110	2	Number of samples per interval
112	4	Zeros
116	8	ASCII word "COMMENT "
124	300	Comment Buffer
424	88	Accumulations

* A hexadecimal number represented as hh.hh . Where hh is a two byte hex number representing either the integer number or the decimal number in 10 thousandths. Ex 10.20 would represent the decimal number 256.0512.

** A hexadecimal number represented as h.h . Where h is a one byte hex number representing either the integer number or the decimal number in tenths.

When the END MILE is reached or the STOP key is pressed

(followed by the ENTER key) the system will write the last summary to tape followed by a file mark to indicate the end of the sequence.

6.6 Printer

The printer is a twenty column serial printer and is driven directly by the microprocessor control unit. It is turned on in the setup menu and is used to print a summary report of the accumulated data associated with each defect category.

6.7 Odometer Circuitry

An odometer which is an automotive industry standard unit, giving approximately 4,000 TTL level positive transitions per mile is required. The actual number of pulses can be anything, the greater the number the more accurate the distance measurements and the greater the number of samples per interval that are possible (within limits). This device must be mounted on the vehicle and can be calibrated by the microprocessor control unit.

6.8 IBM PC/XT Computer System

Please consult the IBM PC/XT system and service manuals for this information. If there are still any questions, call your IBM representative.

SECTION VII
TROUBLESHOOTING

7.1 General

In general the manufacturers manual pertaining to the specific component in question should be referenced when troubleshooting a given problem. The primary components covered in this section are those that have been custom designed and/or built for this piece of equipment.

7.2 Microprocessor Control Unit

When the system is first turned on, the computer goes through a series of checks and tests to check for proper operation of all components. If something is wrong, one or more of the following will happen:

- 1) The microprocessor control unit gives off a constant "beep beep".

Problem: The hand terminal is either not hooked up or else the hand terminal connector is poorly seated. The beeping will stop as soon as the hand terminal is hooked up and functioning properly.

- 2) Hand terminal displays:

The CRP is not
Responding Right
Fl Restart

Problem: The CRP is either not hooked up or else the connector is poorly seated. After checking everything, press the F1 key on the hand terminal to have the system check again.

3) Hand terminal displays:

```
REMOTE TC not  
Connected  
F1 Test Again  
F2 Continue
```

Problem: The Remote Trans. Crack/Odometer input unit is either not hooked up or else the connector is poorly seated. After checking everything press the F1 key on the hand terminal to have the system check again. If you are turning on the system where you don't need the remote transcrack unit (eg. menu familiarization), press F2 on the hand terminal and the system will ignore this problem.

4) Hand terminal displays:

```
Check If Tape Is  
Secured Right  
F1 Restart
```

Problem: The system was either started without a tape in the tape drive or else the tape was not inserted properly. Pull the tape out all the way then firmly push it straight into the tape drive. Press F1 on the hand terminal to check again.

5) Hand terminal displays:

Tape Is Set For
Write Protect
F1 Restart

Problem: The tape cartridge itself is set so that nothing can be written onto the tape. Pull out the tape and first verify that the tape does not already contain information which should not be lost. Then, looking at the top of the tape on the upper left corner, there is a small tab with an arrow pointing to the word "SAFE" Rotate the tab until it points away from the word "SAFE" (180 degrees), reinsert the tape, and press F1 on the hand terminal for the system to check again.

6) Hand terminal display:

Tape Drive Needs
Servicing
F1 Restart

Problem: The tape drive is not properly communicating with the computer. Check for something obvious such as foreign objects in the drive. If pressing F1 on the hand terminal keeps returning you to this message, then the instrument needs to be checked out by a qualified service facility.

7) Hand terminal displays:

Please Toggle The Power

Problem: This usually occurs when the tape drive has been interrupted before fully completing an operation (eg. pulling the tape out in the middle of an active test sequence).

If the system continues to indicate one of the problems mentioned, then the system needs to be checked out by a qualified service facility and servicing should not be attempted while in the field. If a problem occurs that is not mentioned above, check the troubleshooting procedures in the following sections which cover specific items. As a last resort try turning the power on and off and reinitialize the system from the hand terminal.

7.3 Keyboard

Key Replacement

To replace a key, it must be desoldered from the board. Some of the keys are in group of threes. If this is so the entire group will need to be replaced. It can be replaced with another group of three or else three single keys. There is a small slot on the top of the key where the key label may be removed from the old key and inserted into the new one. The mounting holes on the circuit board are polarized so that the keys can be mounted only when positioned the correct way.

Key LED Replacement

To replace a key LED, the switch has to be removed first. When mounting the new LED, be sure that the top of the LED is 3/10 of an inch from the circuit board. This will give the maximum light output and still give enough clearance for switch movement.

Key and Lamp Troubleshooting

Except for continuity checks, the first circuit board (keyboard) should be checked with the second board attached to supply proper voltage levels. Check each LED by supplying +5V to the proper input signal line on the second board.

Logic Board

If the computer indicates that the CRP is not communicating correctly and the connector has been verified to be seated securely, then there is a high probability that the problem is in the logic board. Check both the buffers and the key flip-flops.

7.4 Odometer Circuitry

The odometer circuitry is located on the interface board. If the odometer signal is present at the connector but not effecting the system when it should, verify that the system is enabling the odometer input by placing a high on pin 13 of U3 and that the signal is on pins 11 and 12 of U3.

SECTION VIII

SCHEMATICS, DRAWINGS AND FIGURES

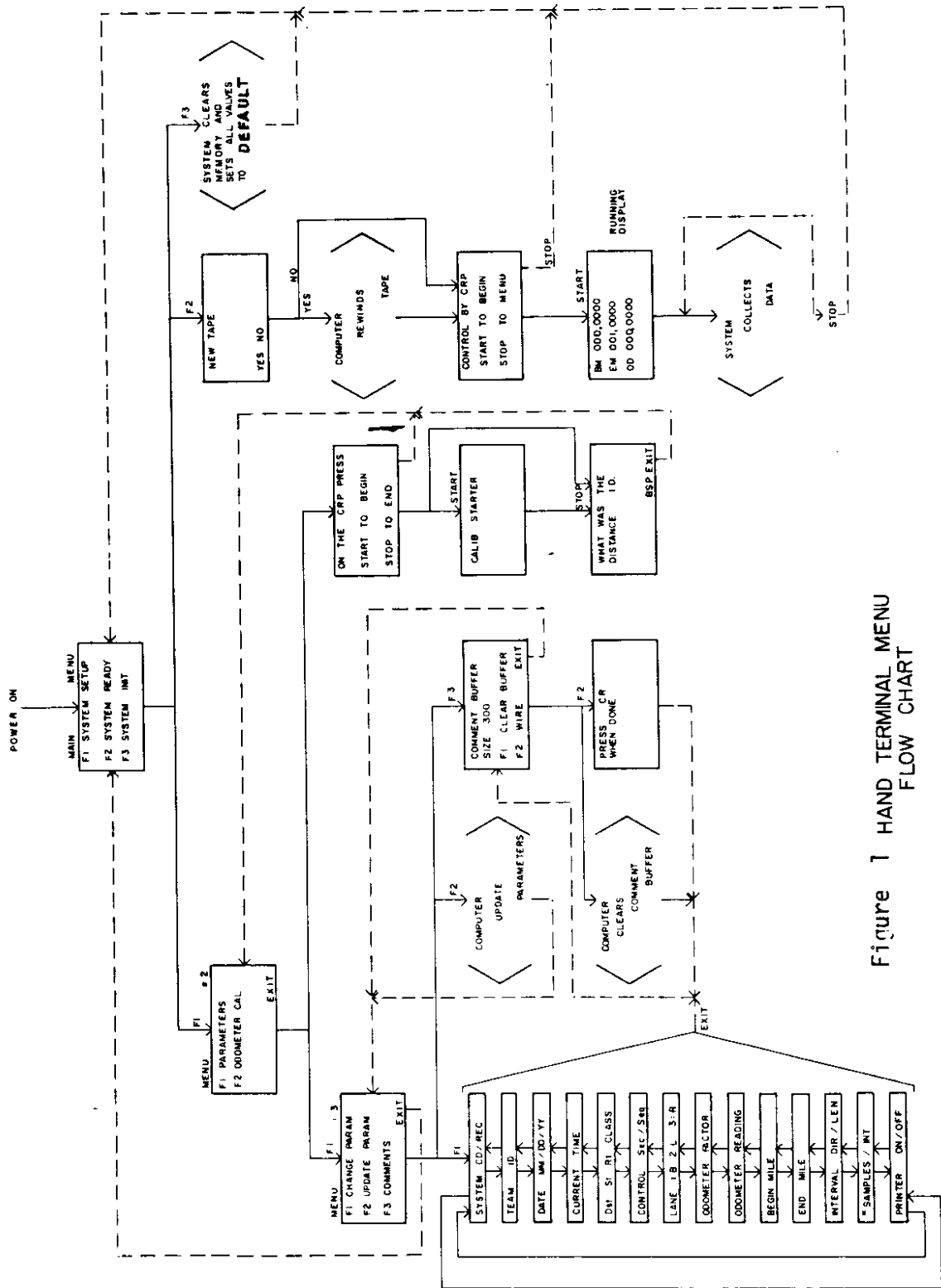


Figure 1 HAND TERMINAL MENU FLOW CHART

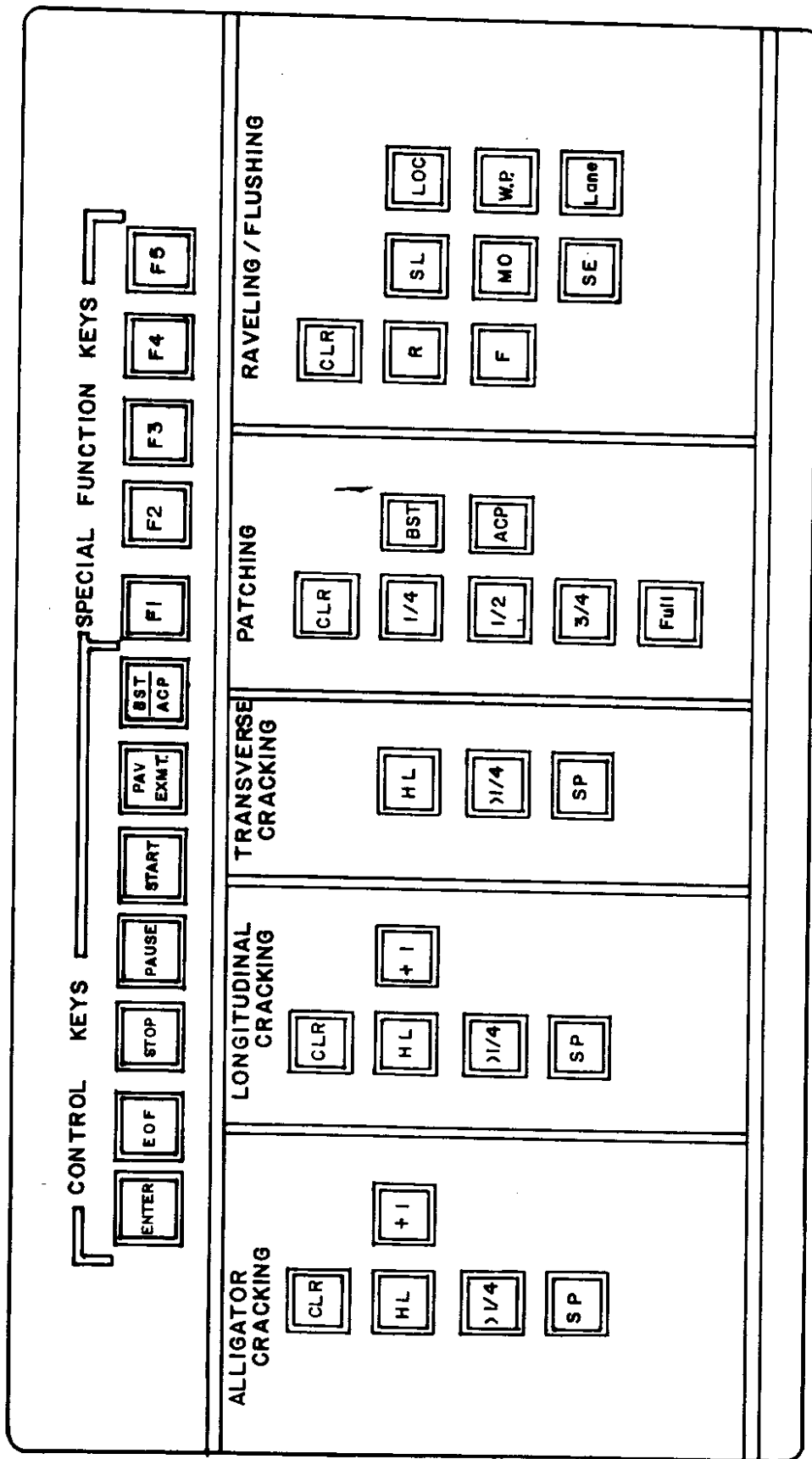


Figure 2 Crp Keyboard Layout

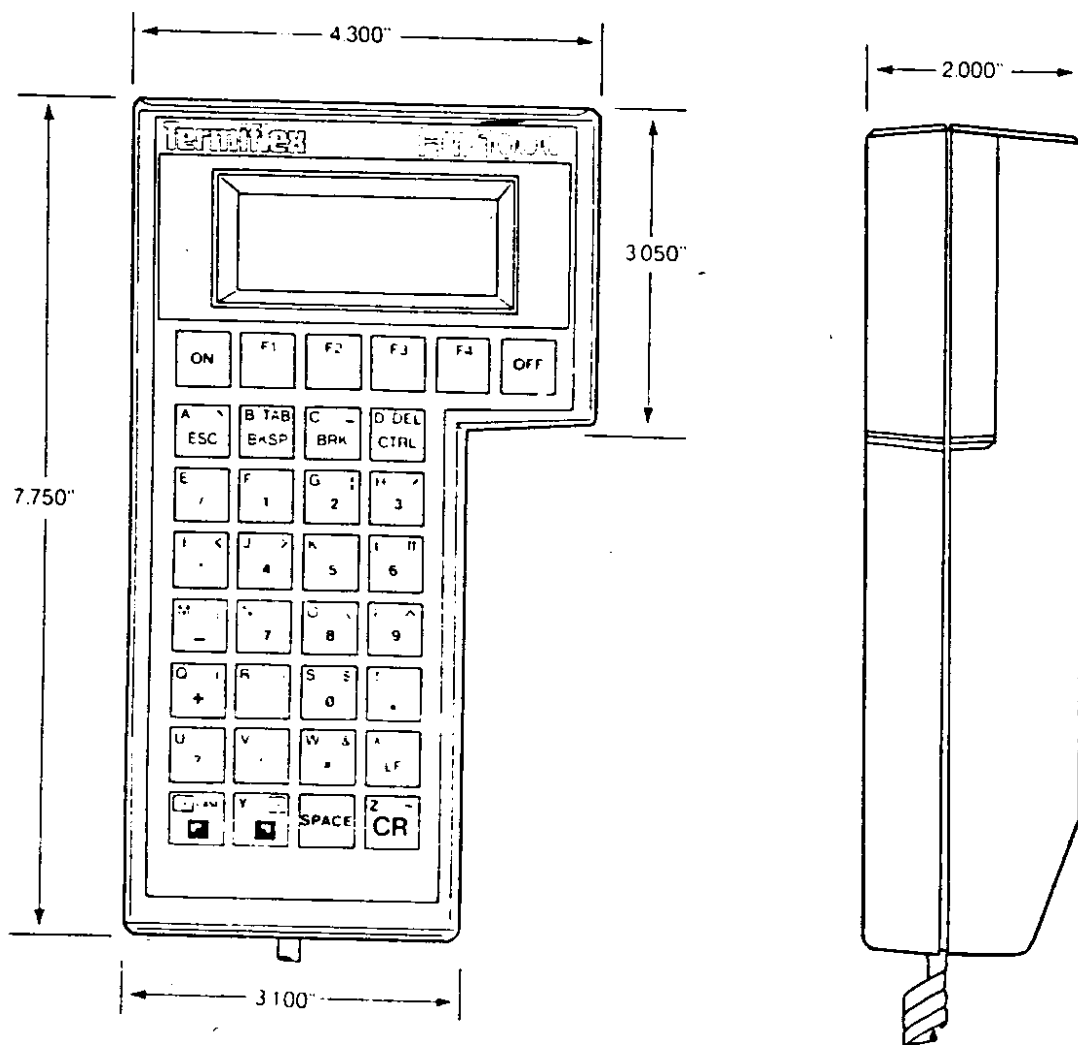


Figure 3 Hand Terminal Layout

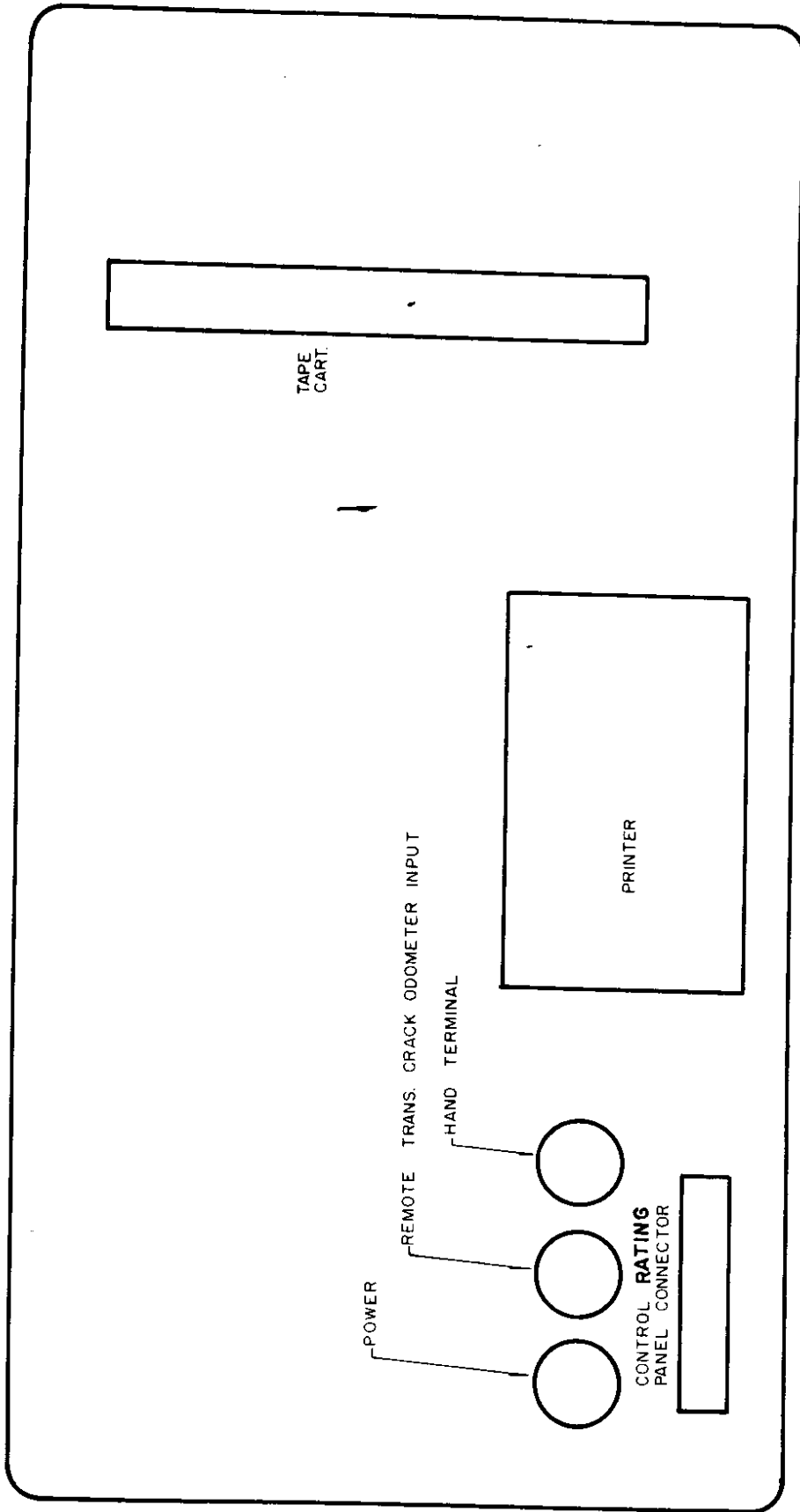
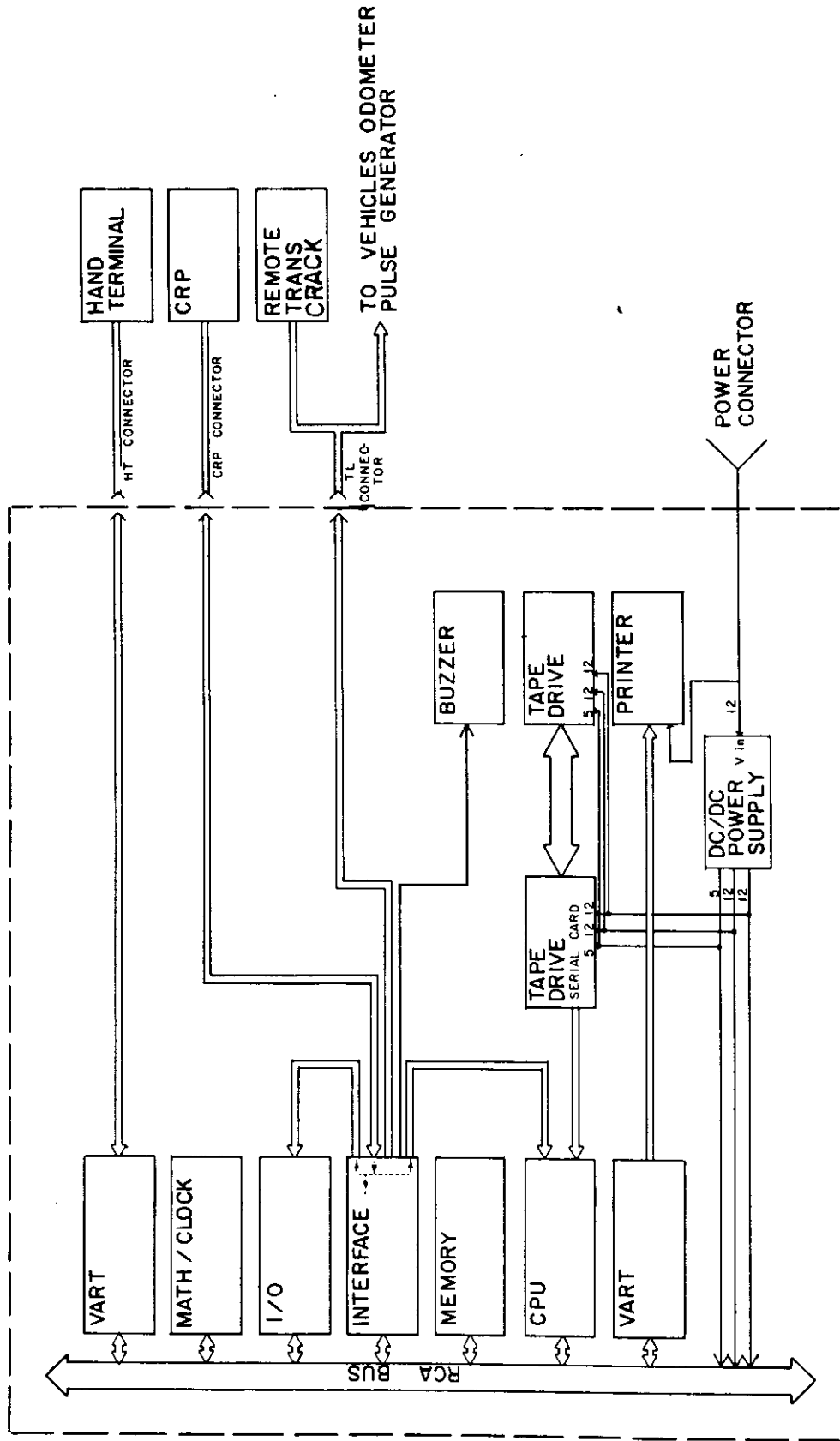
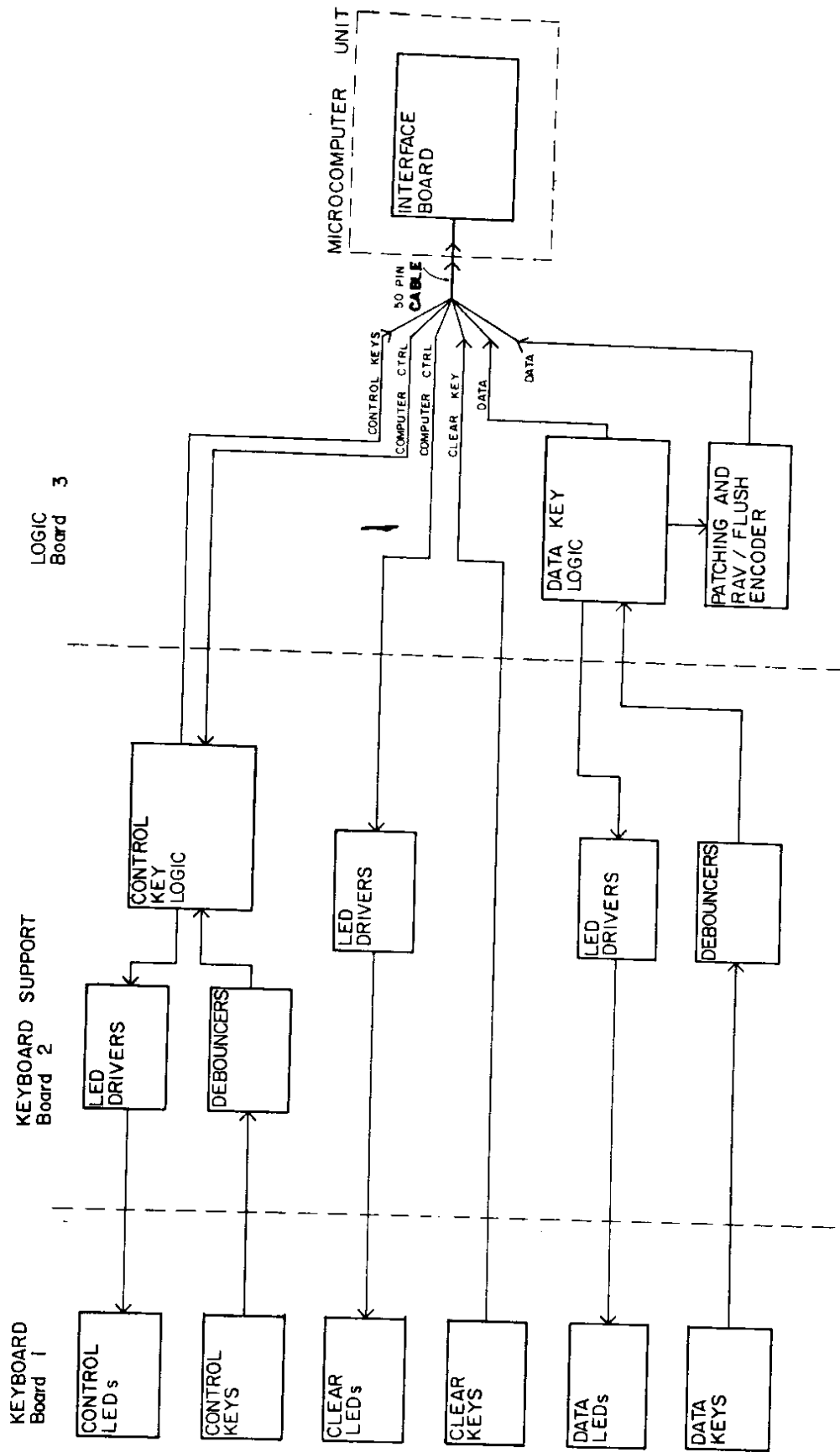


Figure 4 Microcomputer Control Unit Panel Layout



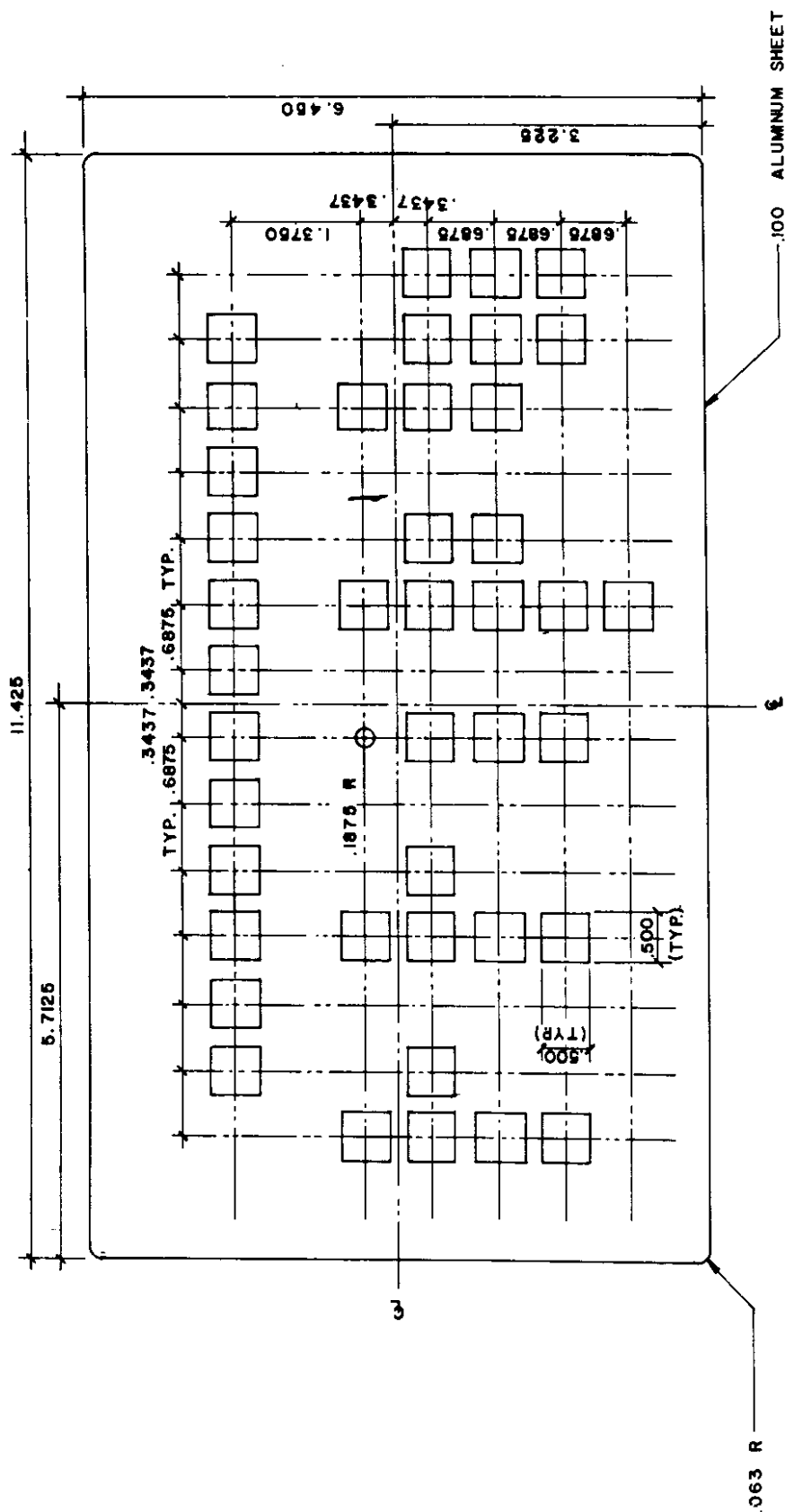
PAVEMENT SURVEY SYSTEM BLOCK DIAGRAM

Figure 5 Pavement Survey System Block Diagram



CRP BLOCK DIAGRAM

Figure 6 CRP Block Diagram



TOP PLATE

NOTE: ALL DIMENSIONS ARE IN INCHES

Figure 7 CRP Keyboard Top Plate Construction Detail

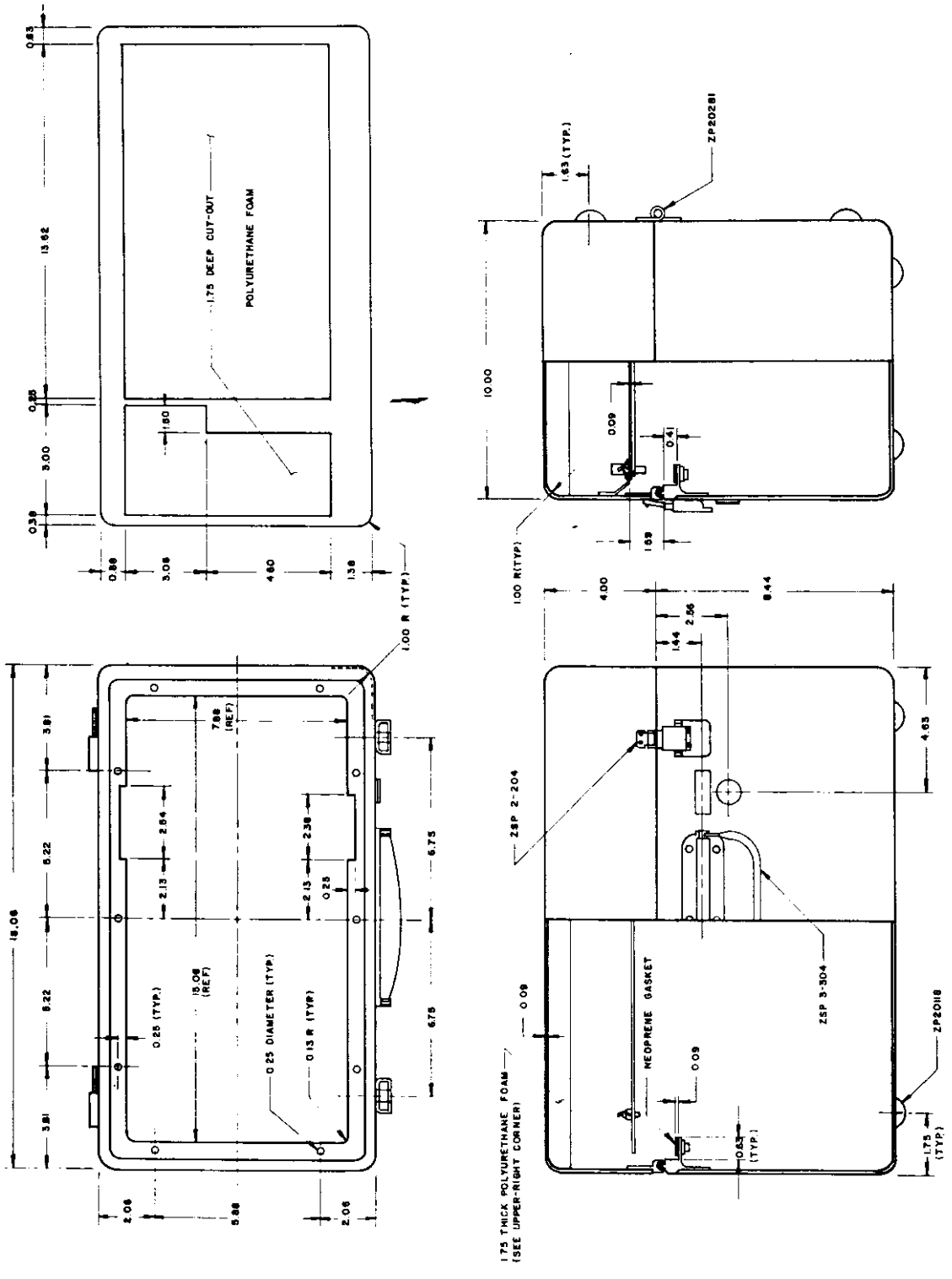
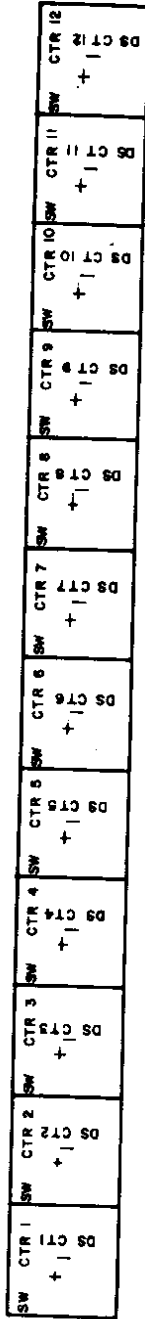


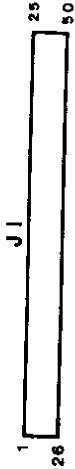
Figure 11 System Enclosure - Construction Detail

CRP KEYBOARD



CLR LED
OP#1 OP#2

1 3 5 7
2 4 6



CLR LED
OP#3 OP#4

8 10 12 14
9 11 13

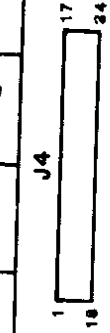
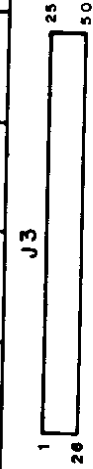
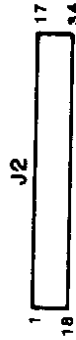
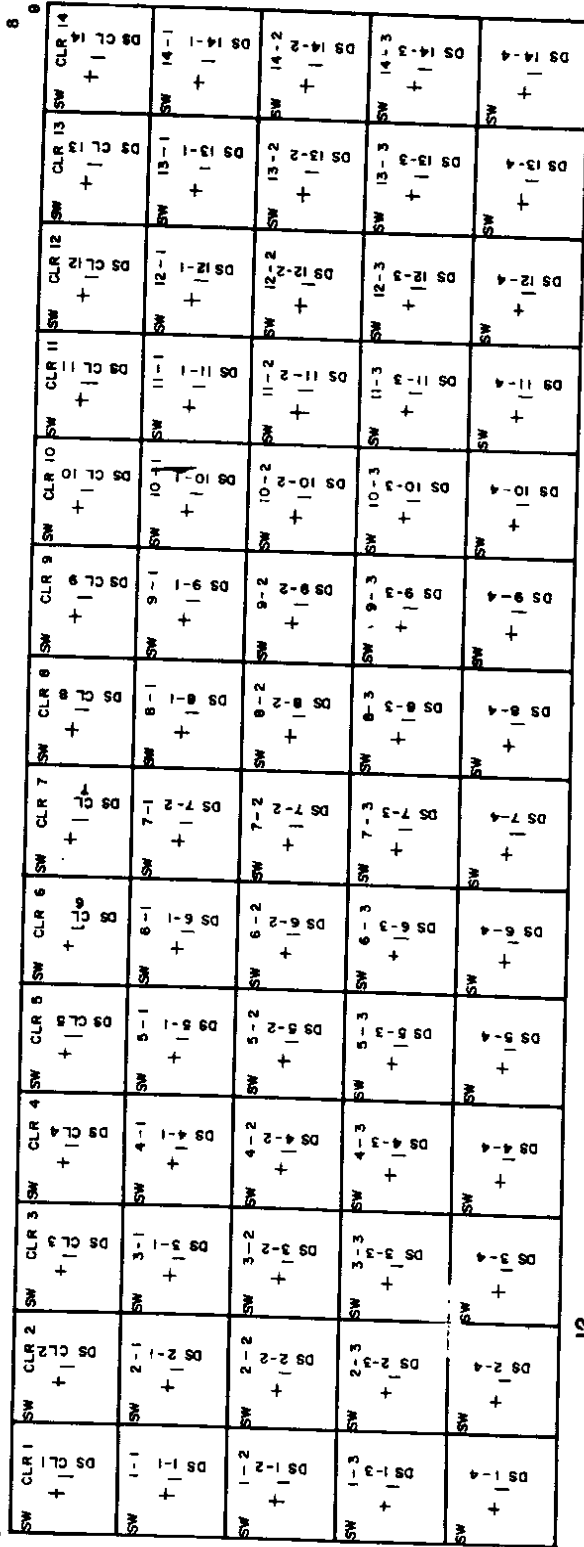


Figure 12 CRP Keyboard PCB Layout - Keyboard

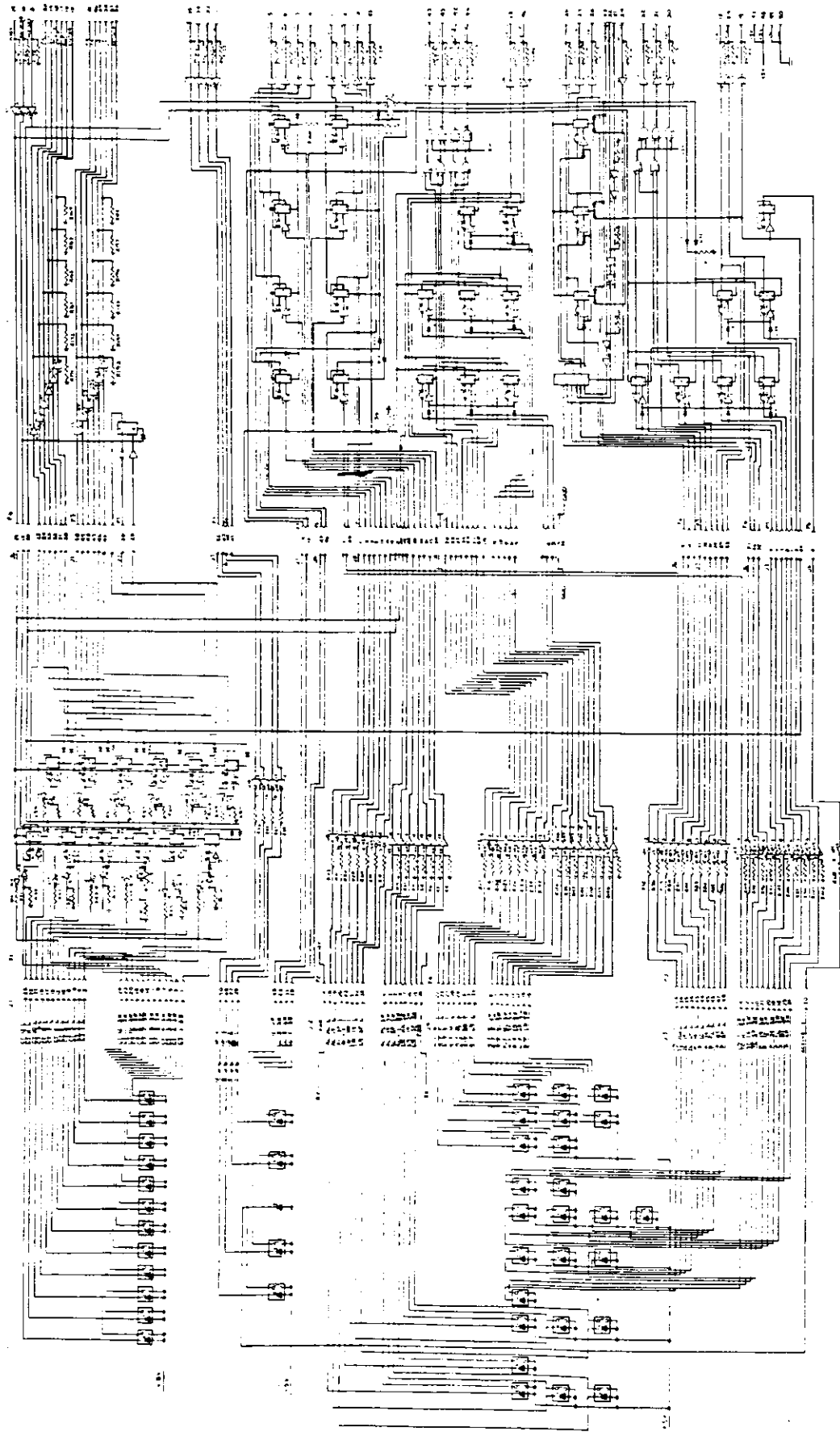


Figure 15 CRP Keyboard - Electronics Schematic

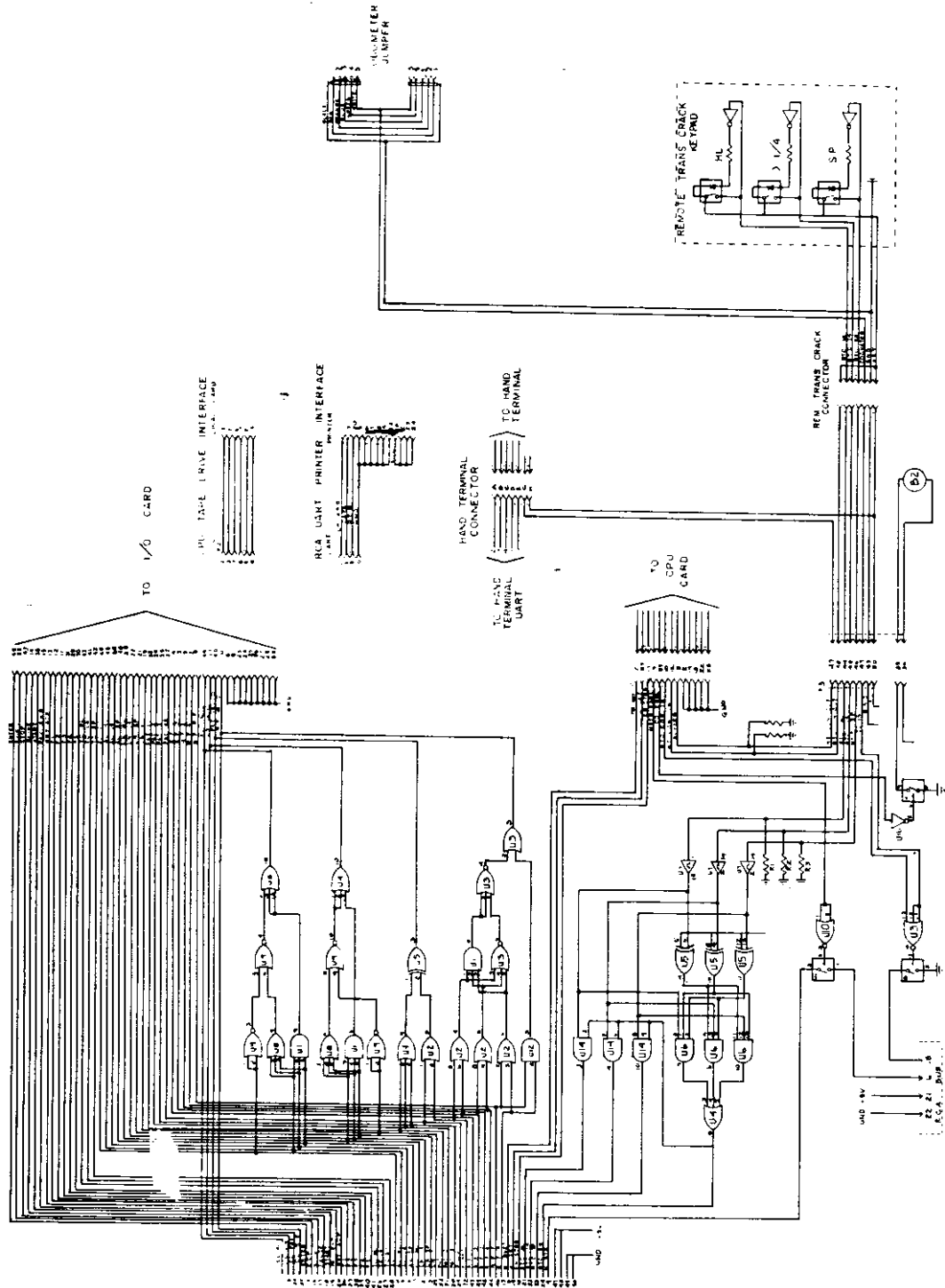


Figure 16 Custom Interface Board and Connector Detail

APPENDIX A
GLOSSARY AND ABBREVIATIONS

AL - Alligator Crack

ACP - Asphalt Concrete Pavement

BM - Beginning mile post.

BST - Bituminous Surface Treatment

CLASS A,B,C - There are three classes of parameters; A) Those parameters which must have a value for the system to run a sequence and are loaded with a default value when the system is initialized; B) Those parameters which are not needed for a successful run of a sequence, but are still loaded with a default value when the system is initialized, and C) those parameters which are used only for information.

CLR - Clear all keys in this section of CRP

CRP - Control-Rating Panel

The hand held keyboard used for entering road fault conditions and controlling basic program execution. Also referred to as the Keyboard.

EM - Ending milepost.

Enter - Used to enter control command on CRP

EOF - End of File

F - Flushing

FULL - Full depth

HL - Hairline

HT - Hand Terminal

F1-F2 - Special Function keys - push-on push-off operation. These keys are counted for each sample until they are released

F3-F4 - Special Function keys - momentary on operation. Reset by the computer each time they are sampled.

Header - Refers to the information put on the tape preceding the actual data record.

Internal Summary - This is the accumulated data summary of the individual surface condition data which is

stored internally on the magnetic tape.

Keyboard - The data entry panel used to enter the surface condition data.

Lane - The actual traffic lane being surveyed.

LOC - Location

LN - Longitudinal Crack

MCU - Microcomputer Control Unit

The main instrument package which houses the computer system, printer, tape drive, and front connectors.

MO - Moderate

PAUSE - Returns control of MCU back to the HT during data sampling.

PAV EXMT - Pavement Exempt

R - Raveling

Record - A 512 byte block of information on the tape which could either be default data, a sequence header, or an interval summary.

RTC - Remote Transverse Crack

The hand held unit containing three push-buttons used for entering transverse crack information remote from the CRP.

R/F - Raveling/Flushing

Sequence

An operator defined section of data on tape which is all the road default data accumulated between the Begin Mile and either the End Mile or the point where the operator pushed the STOP button.

A sequence is always preceded by a 512 byte information header and ended with a file mark on the tape.

STOP - Stops data sampling.

START - Start data sampling.

SE - Severe

SL - Slight

SP - Spalling

TC - Transverse Crack

APPENDIX B

COMPONENT INTERCONNECT DETAILS

The interconnections details between the keyboard and the control unit are given below.

660 BOARD

PIN #	PORT-BIT	ASSIGNED FUNCTION (ALL ARE INPUT)
49	1A-RDY	Control #1 (Enter)
47	1A-STB	Control #3 (Stop)
45	1A-0	Allig. Crack HL
50	1A-1	Allig. Crack >1/4
48	1A-2	Allig. Crack SP
46	1A-3	Allig. Crack +1
44	1A-4	Allig. Valid Data *
43	1A-5	Trans. Crack HL
41	1A-6	Trans. Crack >1/4
42	1A-7	Trans. Crack SP
35	1B-RDY	Control #5 (Start)
33	1B-STB	Control #2 (EOF)
31	1B-0	Control #10 (Flag #3)
29	1B-1	C 1B-2 Control #12 (Flag #5)
32	1B-3	Patching #1
34	1B-4	Patching #2
36	1B-5	Patching #3
37	1B-6	Patching ACP/BST **
40	1B-7	Patching Valid Data *
2	2A-RDY	
1	2A-STB	
4	2A-0	RAV/Flush #1
3	2A-1	RAV/Flush #2
5	2A-2	RAV/Flush #3
7	2A-3	RAV/Flush #4
9	2A-4	RAV/Flush R/F ***
10	2A-5	RAV/Flush Valid Data *
12	2A-6	Control #8 (Flag #1)
11	2A-7	Control #9 (Flag #2)
16	2B-RDY	
18	2B-STB	
20	2B-0	Long. Crack HL
22	2B-1	Long. Crack >1/4
21	2B-2	Long. Crack SP
19	2B-3	Long. Crack +1
17	2B-4	Long. Crack Valid Data *
15	2B-5	Control #6 (Pavement exempt)
14	2B-6	Control #4 (Pause)
13	2B-7	Control #7 (BST/ACP)

* Low = Valid High = Invalid
 ** Low = BST High = ACP
 *** Low = Raveling High = Flushing

RCA P/N CDP - 18S600 BOARD - P-10

PIN #	PORT BIT	GNED FUNCTION	
29	A-RDY	*	OUTPUT
27	A-STB	*	OUTPUT
25	A-0	----- ODOMETER ENABLE	OUTPUT
23	A-1	MASTER SET	OUTPUT
21	A-2	MASTER RESET	OUTPUT
19	A-3	----- MASTER STROBE TO Q LINE ENABLE	OUTPUT
17	A-4	ENTER KEY STROBE	OUTPUT
15	A-5	BUZZER	OUTPUT
13	A-6	*	OUTPUT
11	A-7	*	OUTPUT
9	B-RDY	*	
7	B-STB	*	
5	B-0	*	
3	B-1	*	
1	B-2	*	
4	B-3	*	
6	B-4	*	
8	B-5	*	
10	B-6	REM TC CONNECTED	INPUT
12	B-7	HAND CONTROLLER CONNECTED	INPUT

* NOT ASSIGNED

NOTES

1. When A-3 is low, the CRP can then be strobed by pulsing the Q-Line.
2. When A-0 is low, the 1805 counter can receive clock pulses via the EF-2 line.
3. A-4 is used to clear the ENTER and EOF keys.

CONNECTOR J9

OUTPUT CONNECTOR

PIN #	SIGNAL NAME	REMARKS	SIGNAL DIRECTION
1	Longit. HL	SW 4-1	Out
2	Longit. >1/4	SW 4-2	Out
3	Longit. SP	SW 4-3	Out
4	Allig. +1	SW 2-1	Out
5	Allig. HL	SW 1-1	Out
6	Allig. >1/4	SW 1-2	Out
7	Allig. SP	SW 1-2	Out
8	Master Reset		In
9	Master Strobe		In
10	Enter Strobe	OP#1	In
11	Alligator Valid	OP#2	In
12	Patching BST	OP#3	Out
13	Rav/Flush Rav	OP#4	Out
14	Master Set		In
15	Control #1	CTR-1	Out
16	Control #2	CTR-2	Out
17	Control #3	CTR-3	Out
18	Control #4	CTR-4	Out
19	Control #5	CTR-5	Out
20	Control #6	CTR-6	Out
21	Remote Trans. Crack HL		In
22	Remote Trans. Crack >1/4		In
23	Remote Trans. Crack SP		In
24	Remote Trans. Crack Switching		In
25	Longit. +1	SW 5-1	Out
26	Trans. Crack HL	SW 7-1	Out
27	Trans. Crack >1/4	SW 7-2	Out
28	Trans. Crack SP	SW 7-3	Out
29	Patching ACP	ACP	Out
30	Patching #3	1/4+3/4	Out
31	Patching #2	1/2+3/4	Out
32	Patching #1	Full	Out
33	Longitudinal Valid	OP#5	In
34	Patching Valid	OP#6	In
35	Rav / Flush Valid	OP#7	In
36	Control #7	CTR-7	Out
37	Control #8	CTR-8	Out
38	Control #9	CTR-9	Out
39	Control #10	CTR-10	Out
40	Control #11	CTR-11	Out
41	Control #12	CTR-12	Out
42	RAV/Flush #3	Loc/Lane	Out
43	RAV/Flush #1	SE/SL	Out
44	RAV/Flush #4	Lane/W.P.	Out
45	RAV/Flush #2	SE/MD	Out
46	RAV/Flush Flush	Flush	Out
47	+5 V Power		In
48	+5 V Power		In
49	Ground		In
50	Ground		In

INTERFACE BOARD

	J1 CRP	J2 660 BD.	J3 600 BD.
Pin #1	LN-HL		
2	LN-14		
3	LN-SP		GND
4	AL +1	R/F-2	
5	AL-HL	R/F-1	
6	AL-14	R/F-3	
7	AL-SP	GND	
8	M RSET	R/F-4	
9	M STB	GND	
10	EN-STRB	R/F-R/F	
11	CL-AL	R/F VALID	RTC CON IN
12	P-BST	F2	
13	R/F-R	F1	HT CON IN
14	M SET	BST/ACP	
15	ENTER	PAUSE	GND
16	EOF	PAV EXP	BUZZER
17	STOP		
18	PAUSE	LN-VALID	EN-STRB
19	START		GND
20	PAV EXP	LN+1	M STB
21	RTC-HL	LN-HL	
22	RTC-14	LN-SP	M RSET
23	RTC-SP	LN-14	GND
24	RTC-SW	GND	M SET
25	LN +1	GND	
26	TC-HL	GND	OD ENBL
27	TC-14	GND	
28	TC-SP	GND	GND
29	P-ACP	F4	
30	PAT 3	F5	
31	PAT 2	F3	
32	PAT 1	PAT 1	
33	CL-LN	EOF	
34	CL-PAT	PAT 2	
35	CL-R/F	START	BUZ OUT
36	BST/ACP	PAT 3	+5 V DC
37	F1	PAT-A/B	
38	F2	GND	
39	F3		
40	F4	PAT-VALID	
41	F5	TC-14	
42	R/F-3	TC-SP	
43	R/F-1	TC-HL	GND
44	R/F-4	AL-VALID	RTC-HL (IN)
45	R/F-2	AL-HL	RTC-14 (IN)
46	R/F-FF	AL +1	RTC-SP (IN)
47	+5 V	STOP	HT CON OUT
48	+5 V	AL-SP	RTC CON OUT
49	GND	ENTER	OD (IN)
50	GND	AL-14	+5 V

		CRP CONNECTORS P1/J1 - P4/J4									
P1/J1 50 pin		P2/J2 34 pin		P3/J3 50 pin		P4/J4 34 pin					
pin#											
1	CTR-1	SW						SW	11-4	SW	
2	CTR-1	L-OUT	SW	1-3	SW			SW	11-3	SW	
3	CTR-2	SW	SW	1-2	SW			SW	11-2	SW	
4	CTR-2	L-OUT	SW	1-1	SW	SW	5-1	SW	11-1	SW	
5	CTR-3	SW						SW	12-4	SW	
6	CTR-3	L-OUT						SW	12-3	SW	
7	CTR-4	SW						SW	12-2	SW	
8	CTR-4	L-OUT	SW	2-1	SW			SW	12-1	SW	
9	CTR-5	SW	+5V POWER					NC			
10	CTR-5	L-OUT			SW	7-3	SW	SW	13-4	SW	
11	CTR-6	SW			SW	7-2	SW	SW	13-3	SW	
12	CTR-6	L-OUT			SW	7-1	SW	SW	13-2	SW	
13	NC				NC			SW	13-1	SW	
14	CTR-7	SW						SW	14-4	SW	
15	CTR-7	L-OUT	SW	4-3	SW			SW	14-3	SW	
16	CTR-8	SW	SW	4-2	SW			SW	14-2	SW	
17	CTR-8	L-OUT	SW	4-1	SW			SW	14-1	SW	
18	CTR-9	SW	SW	1-1	L-OUT	SW	9-4	SW	SW	11-1	L-OUT
19	CTR-9	L-OUT	SW	1-2	L-OUT	SW	9-4	SW	SW	11-1	L-OUT
20	CTR-10	SW	SW	1-3	L-OUT	SW	9-2	SW	SW	11-3	L-OUT
21	CTR-10	L-OUT				SW	9-1	SW	SW	11-4	L-OUT
22	CTR-11	SW	SW	2-1	L-OUT	SW	10-4	SW	SW	12-1	L-OUT
23	CTR-11	L-OUT				SW	10-3	SW	SW	12-2	L-OUT
24	CTR-12	SW				SW	10-2	SW	SW	12-3	L-OUT
25	CTR-12	L-OUT				SW	10-1	SW	SW	12-4	L-OUT
26	CRL LED OP#1		+5V POWER			SW	5-1	L-OUT	NC		
27	CRL LED OP#2					SW	5-2	L-OUT	SW	13-1	L-OUT
28	CRL-1	SW				SW	5-3	L-OUT	SW	13-2	L-OUT
29						SW	5-4	L-OUT	SW	13-3	L-OUT
30						SW	6-1	L-OUT	SW	13-4	L-OUT
31	CLR-4	SW	SW	4-1	L-OUT	SW	6-2	L-OUT	SW	14-1	L-OUT
32			SW	4-2	L-OUT	SW	6-3	L-OUT	SW	14-2	L-OUT
33			SW	4-3	L-OUT	SW	6-4	L-OUT	SW	14-3	L-OUT
34						SW	7-1	L-OUT	SW	14-4	L-OUT
35	NC					SW	7-2	L-OUT			
36	NC					SW	7-3	L-OUT			
37	NC					SW	7-4	L-OUT			
38	NC					NC					
39	NC					SW	8-1	L-OUT			
40	NC					SW	8-2	L-OUT			
41	NC					SW	8-3	L-OUT			
42						SW	8-4	L-OUT			
43	CLR-9	SW				SW	9-1	L-OUT			
44						SW	9-2	L-OUT			
45						SW	9-3	L-OUT			
46	CLR-12	SW				SW	9-4	L-OUT			
47						SW	10-1	L-OUT			
48						SW	10-2	L-OUT			
49	CLR LED OP#3					SW	10-3	L-OUT			
50	CLR LED OP#4					SW	10-4	L-OUT			

NOTES D-SW - Output of Debouncer L-OUT - Output of LED Driver
 OUT - Output of F/F SW - Switch output NC - Not connected

		CONNECTORS P5/J5 - P8/J8											
P5/J5 34 pin				P6/J6 50 pin			P7/J7 50 pin			P8/J8 34 pin			
pin#													
1	SW	1-1	OUT	SW	5-1	OUT	SW	10-1	D-SW	SW	14-1	D-SW	
2	SW	1-2	OUT				SW	10-2	D-SW	SW	14-2	D-SW	
3	SW	1-3	OUT							SW	14-3	D-SW	
4													
5	SW	2-1	OUT				SW	9-1	D-SW	SW	13-1	D-SW	
6							SW	9-2	D-SW	SW	13-2	D-SW	
7							SW	9-3	D-SW	SW	13-3	D-SW	
8							SW	9-4	D-SW	SW	13-4	D-SW	
9				SW	7-1	OUT				SW	12-1	D-SW	
10				SW	7-2	OUT				SW	12-2	D-SW	
11				SW	7-3	OUT				SW	12-3	D-SW	
12													
13	SW	4-1	OUT	NC			NC						
14	SW	4-2	OUT	NC			NC						
15	SW	4-3	OUT	ENT STRB IN									
16				ALLIG. VALID			CLR-9	SW					
17	+5V	POWER											
18											GROUND		
19	SW	1-3	D-SW	SET LINE			CLR-12	SW		SW	14-3	OUT	
20	SW	1-2	D-SW	CTR-1	OUT					SW	14-2	OUT	
21	SW	1-1	D-SW	CTR-2	OUT					SW	14-1	OUT	
22				CTR-3	OUT		CLR LED OP#4						
23				CTR-4	OUT		CLR LED OP#3			SW	13-3	OUT	
24				CTR-5	OUT		STROBE LINE			SW	13-2	OUT	
25	SW	2-1	D-SW	CTR-6	OUT		RESET LINE			SW	13-1	OUT	
26													
27													
28													
29							SW	10-2	OUT	SW	12-2	OUT	
30				SW	5-1	D-SW	SW	10-1	OUT	SW	12-1	OUT	
31	SW	4-3	D-SW				SW	9-4	OUT				
32	SW	4-2	D-SW				SW	9-3	OUT				
33	SW	4-1	D-SW				SW	9-2	OUT				
34	+5V	POWER					SW	9-1	OUT				
35											GROUND		
36				SW	7-3	D-SW							
37				SW	7-2	D-SW							
38				SW	7-1	D-SW							
39				NC			NC						
40				NC			NC						
41							SET LINE						
42							LONG.VALID IN						
43							PATCH VALID IN						
44				CLR-4	SW								
45							RAV/FL VALID IN						
46							CTR-7	OUT					
47							CTR-8	OUT					
48				CLR LED OP#1			CTR-9	OUT					
49				CLR LED OP#2			CTR-10	OUT					
50				STROBE LINE			CTR-11	OUT					
				RESET LINE			CTR-12	OUT					

NOTE D-SW - Output of Debouncer L-OUT - Output of LED Driver
 OUT - Output of F/F SW - Switch output NC - Not connected

APPENDIX C

IBM PC/XT SOFTWARE

TDRIV Users Guide

TDRIV is a program designed to read data tapes from the prototype PMS data recorder. In addition to displaying the sequence and interval summaries, TDRIV can display individual samples or compute severity, extent and deduct values for intervals.

Starting TDRIV

TDRIV is located on the hard disk in directory \DOT, so to make running and loading easier, it is usually a good idea to move yourself into this directory before running the program. To change into \DOT, type

```
cd \dot <cr>
```

If, however, you want the files you create while running TDRIV to end up in a directory other than \DOT then you should go to that directory instead and use a different form of the load command discussed below.

Since TDRIV is (presently) written in interpreted BASIC, the first step in running it is to load the BASIC interpreter. This is done with the statement

```
basic /c:1000 /s:1000 <cr>
```

where <cr> indicates a carriage return. You should now see a welcome message from BASIC. Next type

```
load "tdriv.bas" <cr>
```

from within directory \DOT or

```
load "c:\dot\t driv.bas" <cr>
```

from any other directory. You should see an "Ok," prompt when this is completed.

To actually start the program, simply type

```
run <cr>
```

TDRIV's opening menu should now appear.

When you are done running TDRIV and are back at the BASIC command level (the "Ok," prompt) type

```
system <cr>
```

to return to PC-DOS.

Running TDRIV

All of the functions in TDRIV are accessed from a main menu. (the one that comes up when the program is first started) The following sections will cover each option in detail.

1) set track

The cartridge tapes are formatted such that there are four logical tracks per tape. The set track function changes the track that the tape drive looks at and hence provides an easy way to skip a quarter of the tape at a time. One word of warning though, the tracks are arranged on the tape in a serpentine fashion so that the end of track one is at the beginning of track two, etc. This means that if you are at the beginning of track one and switch to track two, you will be at the very end of track two and doing any sort of read operation will push you over onto track three.

2) rewind tape

This will move to the beginning of track one and read the first sequence header, positioning you at sequence one, interval one.

3) search for summary

This will search through the tape sequentially from the current position looking for either the next interval summary record or a specific summary, if you gave it an interval number. This is a handy way to move long distances forward in a sequence.

One current problem involves trying to search past a tape error. The drive's search routine will return an error code and leave the tape positioned before the error, so that resubmitting the search will only reveal the same error. As of now, no simple way has been found to gain access to data in a sequence that was recorded after a tape error occurred

4) read current header

This will read the current sequence header. If the tape is currently positioned in the first sequence then this command behaves exactly like (2) rewind. Its main use occurs when the tape is positioned on some sequence other than the first. It can then be used either to recover from a "tape position lost" error without losing track of what sequence it was on or as a fast way to back up. As an example, if the current position was sequence 5, interval 40 (S5I40) and you wanted to move to interval 20 in the same sequence (S5I20) the fastest way to do it would be to (4) read the current header and then (3) search for summary number 20.

5) dump interval to disk

This will dump all the data for a single interval to a disk file of the users choice, one sample per line.

6) display individual samples

This option allows you to see which buttons were depressed for each sample during an interval. The samples are displayed 20

at a time, with blanks representing no data, question marks representing invalid data and various mnemonic symbols (such as Sp for spalling, etc.) representing valid data. After each screen of data you may enter either a carriage return to see the next 20 samples, a specific sample number to see 20 samples starting with that one, or a minus one (-1) to return to the main menu. You will be returned to the main menu automatically when all samples in an interval have been displayed.

7) space forward interval

8) reverse space interval

The forward/reverse space interval function will reposition the tape to the end of the following/preceding interval and then display the interval summary. Should the end/beginning of a sequence be encountered, the sequence header will be read.

9) compute summary statistics

This will compute the severity, extent and deduct values for the current interval, and then display them to the screen following the interval summary.

10) forward space sequence (file)

11) reverse space sequence

The forward/reverse space sequence function moves to the beginning of the following/preceding sequence and reads and displays the sequence header.

12) retension tape

Spins the tape cartridge from one end to the other to even out tape tension. This can sometimes cure intermittent tape errors, if the tape has been sitting for a while or has undergone a great deal of stop and start motion.

13) autosummary of current sequence

This function computes severities, extents and deduct values for all intervals in the current sequence and writes the data into two files. The files names are

<type><state_route><dir><beg_mile>.DAT

where <type> is either H or D for header and data files respectively, <state_route> is the state route number, <dir> is the direction of travel (either P or M for increasing or decreasing mile number) and <beg_mile> is the beginning milepost number. These two files are the two required for input to dBase for later manipulation.

14) stop

Stops the program and returns you to the basic command level.

Common Errors and Problems

Probably the most common error is caused by the tape drive not being awake. If the tape drive has not been used since it has been turned on (the SELECT light is off), TDRIV will probably halt with an "I/O error in 550" message. The cause of this error has not been determined, but its occurrence causes the SELECT light to go on and hence prevents its repetition. Just type run again to restart the program and all should work well.

Another common problem is the program "hanging" and not returning to the menu on the first function selected. This is most likely caused by the tape drive being turned off or a connector having fallen off. Press CTRL and BREAK at the same time to halt the program, then check the switches and connectors before trying again.

Another error manifests itself with an "Illegal function call in 35" message. This probably means that you forgot the "/c:1000 /s:1000" parameters on the BASIC invocation.

DBASE program documentation

To load data files into dBase for the very first time, from within dBase type

```
do load <cr>
```

and answer the questions.

To load the .DBF files back into dBase at a later time, type

```
clear databases
```

```
select1
use H_____ alias header
select 2
use D_____ alias sevext
select 3
use A_____ alias aved
```

where the last two lines load the averaged data base and are completely optional.

To average severity and extent values over intervals and store the results in another database, type.

```
do ave <cr>
```

and answer the questions.

Path: \WPROS Wordstar word processor (overlay files must be in your current directory as well)
Sub-directories: None Also contains document files

Path: \FOR Microsoft FORTRAN (plus working versions of INTERP, etc.)
Sub-directories: None

Path: \UTIL General purpose homebrew utilities
Sub-directories: None

Path: \F77 DRI FORTRAN77 compiler
Sub-directories: None

SOFTWARE LISTINGS - IBM - PC/XT Interface and Tape Drive

```

10 DEFINT A-Z
15 PRINT "program TDRIV for reading pavement survey tapes"
20 REM when entering basic, type basic /c:1000 /s:1000
25 DIM RBUF(600) : NRPERF=0 :CURREC=-1
30 S=512
35 OPEN "com1:9600,n,8,2,rs,cs,ds" AS #1 LEN=S+4
40 REM preset track and pa
45 TRACK = 1 : PA = 0
50 PRINT:PRINT:PRINT " 1 set track"
55 PRINT " 2 rewind tape"
60 PRINT " 3 search for summary"
65 PRINT " 4 read current header"
70 PRINT " 5 dump interval to disk"
75 PRINT " 6 display individual samples"
80 PRINT " 7 space forward interval"
85 PRINT " 8 reverse space interval"
90 PRINT " 9 compute summary statistics"
95 PRINT "10 forward space sequence (file)"
100 PRINT "11 reverse space sequence"
103 PRINT "12 retension tape"
104 PRINT "13 autosummary of current sequence"
105 PRINT "14 stop"
110 INPUT "enter choice ",MENU:PRINT
115 IF MENU > 14 OR MENU < 1 THEN PRINT "***invalid entry": GOTO 50
120 IF MENU = 14 THEN PRINT "goodbye": STOP
125 ON MENU GOSUB 1000,2000,3000,4000,5000,6000,7000,8000,9000,10000,11000,12000,13000
130 GOTO 50
300 REM code to do fake floating point to ASCII conversion
305 DEF FNITOA$(I) = CHR$(I + ASC("0"))
310 FLTSTRG$ = " .0000"
312 IF RBUF(PTR) > 127 THEN MID$(FLTSTRG$,1,4)="????" : GOTO 337
315 ITEMP = 256*RBUF(PTR) + RBUF(PTR+1)
320 IVAL=ITEMP MOD 10: MID$(FLTSTRG$,4) = FNITOA$(IVAL)
325 IVAL = (ITEMP\10) MOD 10: IF ITEMP > 9 THEN MID$(FLTSTRG$,3)=FNITOA$(IVAL)
330 IVAL=(ITEMP\100) MOD 10: IF ITEMP > 99 THEN MID$(FLTSTRG$,2)=FNITOA$(IVAL)
335 IVAL=(ITEMP\1000) MOD 10:IF ITEMP > 999 THEN MID$(FLTSTRG$,1)=FNITOA$(IVAL)
337 IF RBUF(PTR+2) > 39 THEN MID$(FLTSTRG$,6,4)="????" : GOTO 370
340 ITEMP= 256*RBUF(PTR+2) + RBUF(PTR+3)
345 IVAL = ITEMP MOD 10 : MID$(FLTSTRG$,9) = FNITOA$(IVAL)
350 IVAL=(ITEMP\10) MOD 10: IF ITEMP > 9 THEN MID$(FLTSTRG$,8)=FNITOA$(IVAL)
355 IVAL=(ITEMP\100) MOD 10: IF ITEMP > 99 THEN MID$(FLTSTRG$,7)=FNITOA$(IVAL)
360 IVAL=(ITEMP\1000) MOD 10: IF ITEMP >999 THEN MID$(FLTSTRG$,6)=FNITOA$(IVAL)
370 RETURN
400 REM routine to read a record and handle E0Track
410 CA = 1 : GOSUB 500
420 IF ECODE = 0 THEN RETURN
430 IF (DS AND 4) = 0 THEN RETURN
440 IF TRACK < 4 THEN TRACK=TRACK+1 :GOTO 410
450 RETURN

```

```

500 REM routine to talk to the tape drive
505 MA=(TRACK-1) OR &H80
506 IF S=1024 THEN II=&H0 ELSE IF S=2048 THEN II=&H10 ELSE IF S=3072 THEN II=&H20 ELSE IF S=4096 THEN II=&H30 ELSE IF S=8192 THEN II
S=512:II=&H50
507 MA = MA OR II
510 POKE VARPTR(#1)+188,MA
515 POKE VARPTR(#1)+189,PA
520 POKE VARPTR(#1)+190,CA
525 PUT #1,3
530 IF CA (>) 11 THEN GOTO 550
535 FOR II=1 TO 16
540 POKE VARPTR(#1)+187+II, ASC(MID$(MASK$,II,1)) : NEXT II
545 POKE VARPTR(#1)+187+17,191 : PUT #1,17
550 GET #1,2
555 DS=PEEK(VARPTR(#1)+188)
560 IS=PEEK(VARPTR(#1)+189)
565 IF IS AND 48 THEN ECODE=1 ELSE ECODE=0
570 PRINT: PRINT USING "####";"ds = ",HEX$(DS),"h is = ",HEX$(IS),"h"
575 IF ECODE (<) 0 THEN PRINT USING "####"; "ecode = ",ECODE,"d"
580 PRINT
585 RETURN
600 REM routine to read data
610 GET #1,S
620 TPTR=VARPTR(#1)+187
630 FOR II=1 TO S
640 RBUF(II)=PEEK(TPTR+II)
650 NEXT II
660 RETURN
675 REM routine to clear com buffer
680 IF LOC(1)=0 THEN RETURN
685 GET #1,LOC(1)
690 GOTO 680
700 REM this routine will forward space SPCNT records, come hell, high water
705 REM or end of track. Errors are returned with SPCNT = -1
710 IF SPCNT<0 THEN PRINT "***Error, negative space count":RETURN
715 WHILE SPCNT > 0
720 CA=4 : GOSUB 500 'forward space record
725 IF ECODE = 0 THEN GOTO 760 'if no errors then jump
730 IF (DS AND 64) = 0 THEN GOSUB 900:SPCNT=-1:RETURN 'unrecoverable error
735 IF (DS AND 4) = 0 THEN GOTO 750 'jump on NOT end of track
740 IF TRACK < 4 THEN TRACK=TRACK+1 :GOTO 720
745 PRINT "***end of tape!***":SPCNT=-1:RETURN
750 PRINT "***Unexpected filemark!***": GOSUB 4080 :SPCNT=-1:RETURN
760 SPCNT=SPCNT-1
765 WEND
770 RETURN
800 REM routine to reverse space SPCNT records, similar to above
805 IF SPCNT<0 THEN SPCNT=-1: PRINT "***Error, negative space count":RETURN
810 WHILE SPCNT > 0
815 CA=6 : GOSUB 500 'reverse space record
820 IF ECODE = 0 THEN GOTO 860 'if no errors then jump
825 IF (DS AND 64) = 0 THEN GOSUB 900:SPCNT=-1:RETURN 'unknown type error
830 IF (DS AND 8)=0 THEN GOTO 845 'jump if not BOTrack
835 IF TRACK >1 THEN TRACK=TRACK-1 :GOTO 815
840 PRINT "***beginning of tape!***":SPCNT=-1:GOSUB 4500 :RETURN
845 PRINT "***unexpected filemark***" 'so step forward and read header

```

```

850 CA=4 : GOSUB 500 : GOSUB 4080 : SPCNT=-1: RETURN
860 SPCNT=SPCNT-1
865 WEND
870 RETURN
900 REM routine to issue discouraging message and damage global variables
910 PRINT
920 PRINT "***Tape Position Lost***"
930 PRINT "(next command must be either search, rewind or a file command)"
940 PRINT
950 CURREC=-1
960 GOSUB 675 'clear comm buffer
970 RETURN
1000 REM routine to set track on tape drive
1010 PRINT
1020 PRINT "current track is",TRACK
1030 INPUT "enter new track";TEMP
1040 IF (TEMP < 1) OR (TEMP > 4) THEN PRINT : PRINT "***invalid track",TEMP : GOTO 1010
1045 TRACK = TEMP
1050 CURREC = -1
1060 RETURN
2000 REM routine to rewind tape
2010 TRACK = 1
2020 CA = 72 'send status bytes relative to B0Tape
2030 GOSUB 500
2040 PRINT
2060 GOSUB 4080 'read the first header record
2070 RETURN
3000 REM routine to search for and display a summary record
3005 INPUT "enter a specific interval number or <CR> for next summary"; INTNO
3010 MASK$ = "SUMMARY ????????"
3015 IF INTNO > 0 THEN MID$(MASK$,9,2)=CHR$(INTNO\256)+CHR$(INTNO MOD 256)
3020 PRINT :FOR I=1 TO 16: PRINT HEX$(ASC(MID$(MASK$,I,1))); : NEXT I
3025 PRINT " ";
3030 FOR I=1 TO 16
3031 J=ASC(MID$(MASK$,I))
3032 IF ((J>31) AND (J<127)) THEN PRINT CHR$(J); ELSE PRINT ".";
3033 NEXT I
3035 HEADSUM$="SUM": PRINT
3040 CA = 11 : GOSUB 500 'search for record
3045 IF DS AND 64 THEN PRINT "***filemark detected":GOSUB 4080:RETURN
3050 IF ECODE (<) 0 THEN GOSUB 900 : RETURN 'abort if unable to read
3055 GOSUB 600 'load into rbuf()
3200 TITLE$=" " : FOR CPTR=1 TO 8
3205 MID$(TITLE$,CPTR) = CHR$(RBUF(CPTR))
3210 NEXT CPTR
3215 MISPOS=0 : CURREC = NRPERF+2
3220 IF TITLE$ = "SUMMARY " THEN GOTO 3400
3225 MISPOS=-1 : CURREC = -1
3230 PRINT USING "###"; "***expecting 'SUMMARY ', found '",TITLE$,""
3235 GOSUB 900 : RETURN 'scream and die
3400 RECOMP=0 ' flag for what to display
3405 DEF FNCR$(JJ)=CHR$(RBUF(JJ))
3410 NULL$=" " : DSH$="-" : WS$="WS" : DOT$="." : CS$="," : EP$="!"
3415 FORM0$="#####!"
3420 FORM1$="#####!###": FORM2$="& !! !": FORM3$="&##!##!##": FORM4$="& #!###!##"

```



```

3685 LSET F$="# times flag 2 on": PRINT USING FORM1$,F$,NULL$,F2
3690 IF RECOMP=0 THEN F3=256*RBUF PTR)+RBUF PTR+1) : PTR=PTR+2
3695 LSET F$="# times flag 3 on": PRINT USING FORM1$,F$,NULL$,F3
3700 IF RECOMP=0 THEN F4=256*RBUF PTR)+RBUF PTR+1) : PTR=PTR+2
3705 LSET F$="# times flag 4 on": PRINT USING FORM1$,F$,NULL$,F4
3710 IF RECOMP=0 THEN F5=256*RBUF PTR)+RBUF PTR+1) : PTR=PTR+2
3715 LSET F$="# times flag 5 on": PRINT USING FORM1$,F$,NULL$,F5
3720 IF RECOMP=1 THEN PTR=PTR+10
3725 PRINT: F$=SPACE$(52): LSET F$="Transverse crack count HL"
3730 IF RECOMP = 1 THEN PRINT USING FORM1$, F$,NULL$,TCN1 ELSE PRINT USING FORM1$, F$,NULL$,RBUF PTR)*256+RBUF PTR+1)
3735 PTR=PTR+2
3740 LSET F$="                )1/4"
3745 IF RECOMP = 1 THEN PRINT USING FORM1$, F$,NULL$,TCN2 ELSE PRINT USING FORM1$, F$,NULL$,RBUF PTR)*256+RBUF PTR+1)
3750 PTR=PTR+2
3755 LSET F$="                SP"
3760 IF RECOMP = 1 THEN PRINT USING FORM1$, F$,NULL$,TCN3 ELSE PRINT USING FORM1$, F$,NULL$,RBUF PTR)*256+RBUF PTR+1)
3765 PTR=PTR+2
3770 N1=RBUF PTR)*256+RBUF PTR+1):PTR=PTR+2
3775 N2=RBUF PTR)*256+RBUF PTR+1):PTR=PTR+2
3780 N3=RBUF PTR)*256+RBUF PTR+1):PTR=PTR+2
3785 F$="Comments: "
3790 PRINT USING FORM6$, F$;
3795 WHILE (PTR < S) AND (RBUF PTR) <> 26)
3800 PRINT USING FORM6$, CHR$(RBUF PTR));
3805 PTR=PTR+1
3810 WEND
3820 PRINT CHR$(13); CHR$(10);
3825 INPUT "enter (cr) to continue",I
3830 RETURN
4000 REM routine to read the current header and display it
4010 CA=7
4020 GOSUB 500 'reverse to filemark
4030 IF ECODE = 0 THEN GOTO 4070 'jump if no errors
4040 IF (DS AND 8) = 0 THEN GOSUB 900:RETURN 'abort if confused
4050 IF TRACK > 1 THEN TRACK = TRACK - 1 :GOTO 4010
4060 GOTO 4080
4070 CA=4 : GOSUB 500 'step over filemark
4080 REM entry point for many other routines that want to read a header
4085 CA=1 : GOSUB 500 'read header
4090 IF ECODE = 0 THEN GOTO 4130
4100 IF (DS AND 4) = 0 THEN GOSUB 900 : RETURN 'abort if error is not E0Track
4110 IF TRACK < 4 THEN TRACK=TRACK+1 : GOTO 4080 'inc track and try again
4120 GOSUB 900 :RETURN 'if we can't figure out what kind of error it was, abort
4130 GOSUB 600 'load header into rbuf()
4500 REM test to see if this is indeed a header record
4510 MISPOS=0 : TITLE$=" "
4520 FOR CPTR=1 TO 8
4530 MID$(TITLE$,CPTR)=CHR$(RBUF(CPTR))
4540 NEXT CPTR
4550 IF TITLE$ = "HEADER " THEN GOTO 4580
4560 PRINT USING "###";"***expecting 'HEADER ', found '",TITLE$,"'"
4570 MISPOS=-1 : GOSUB 900 :RETURN 'crap out and die
4580 REM now we know this is a header, so determine NRPERF and pretend
4590 REM that it's a summary for the purposes of displaying it.
4600 NRPERF = RBUF(9)

```

```

4605 NSAMP = 256*RBUF(10) + RBUF(11)
4607 IF AUTOSUM=1 THEN CURREC=1: RETURN 'thats all we want for autosummary
4610 HEADSUM$="HEAD"
4620 GOSUB 3400 ' go to summary displaying routine with early return flag set
4630 CURREC=1
4640 PRINT : PRINT : INPUT "hit (CR) to continue",I
4650 RETURN
5000 REM routine to write data from a single interval to disk
5010 IF CURREC < 0 THEN GOSUB 900 : RETURN
5020 SPCNT = CURREC - 1
5030 GOSUB 800 'back space to first data record
5035 IF SPCNT <> 0 THEN GOSUB 900 : RETURN
5040 INPUT "enter the output file name ",FAME$
5050 OPEN FAME$ FOR OUTPUT AS #2
5060 CURREC = 1 : J = NRPERF+1
5070 IF CURREC=J THEN PRINT "write completed with ",CURREC-1," records": GOTO 5200
5080 CA = 1 : GOSUB 500 'read record
5090 IF ECODE()0 THEN GOTO 5150 'jump on error
5100 GOSUB 600 'load data into rbuf
5105 IF CURREC<NRPERF THEN N=S ELSE N=(NSAMP*4) MOD S
5110 FOR I=1 TO N STEP 4
5120 PRINT #2, USING "### ### ### ###"; RBUF(I),RBUF(I+1),RBUF(I+2),RBUF(I+3)
5130 NEXT I
5140 PRINT "record #",CURREC,"written" : CURREC=CURREC+1 : GOTO 5070
5150 REM cleanup code for read errors
5160 PRINT "***read error on tape, disregarding record #",CURREC
5170 GOSUB 675 'clear buffer
5180 CURREC=CURREC+1 : GOTO 5070
5200 REM code to close files and go home
5210 CLOSE #2
5220 RETURN
6000 REM routine to display individual samples
6005 IF CURREC = -1 THEN GOSUB 900 : RETURN
6010 SPCNT=CURREC-1 : GOSUB 800 : CURREC=1 'reverse to first data record
6015 IF SPCNT <> 0 THEN GOSUB 900 :RETURN 'abort if unable to position
6017 PTR = 1
6020 IF CURREC > NRPERF THEN RETURN
6025 GOSUB 400 'read record
6030 IF ECODE (<) 0 THEN RETURN 'abort if unable to read
6035 GOSUB 600 'load
6040 CURREC = CURREC + 1
6045 MORE=1
6050 I=1:PRINT "Sam. | Allig. | Longit. | Trans. | Patching | Rav/Flush | Pav | BST/ | Flags"
6055 PRINT " # | | | | | | | | | | Ex | ACP |"
6060 PRINT " | | | | | | | | | | | | |"
6065 NSAM=((CURREC-2)*128+(PTR-1)/4)+1: BYTE1A=RBUF(PTR): BYTE1B=RBUF(PTR+1)
6070 BYTE2A=RBUF(PTR+2) :BYTE2B=RBUF(PTR+3)
6075 REM code to display information to screen
6080 A$="| | | | | | | | | | | | |"
6085 IF BYTE1A AND 1 THEN MID$(A$,5,1)="H" 'alligator cracks
6090 IF BYTE1A AND 2 THEN MID$(A$,6,1)=")"
6095 IF BYTE1A AND 4 THEN MID$(A$,7,1)="S"
6100 IF BYTE1A AND 8 THEN MID$(A$,8,1)="+"
6105 IF BYTE1A AND 16 THEN MID$(A$,5,4)="????"
6110 IF BYTE2B AND 1 THEN MID$(A$,14,1)="H" 'longitudinal cracks

```

```

6115 IF BYTE2B AND 2 THEN MID$(A$,15,1)=")"
6120 IF BYTE2B AND 4 THEN MID$(A$,16,1)="S"
6125 IF BYTE2B AND 8 THEN MID$(A$,17,1)="+"
6130 IF BYTE2B AND 16 THEN MID$(A$,14,4)="????"
6135 REM transverse cracks
6140 TEMP = BYTE1A AND 224
6145 IF TEMP = 0 THEN MID$(A$,24,1)=" " ELSE IF TEMP = 32 THEN MID$(A$,24,4)="H.L." ELSE IF TEMP = 64 THEN MID$(A$,24,4)="1/4" ELSE
6150 REM patching
6155 TEMP=(BYTE1B \ 8) AND 7 'isolate three bits
6160 IF TEMP = 1 THEN MID$(A$,33,3)="1/4" ELSE IF TEMP = 2 THEN MID$(A$,33,3)="1/2" ELSE IF TEMP = 3 THEN MID$(A$,33,3)="3/4" ELSE I
6165 IF BYTE1B AND 64 THEN MID$(A$,38,1)="A" ELSE MID$(A$,38,1)="B"
6170 IF BYTE1B AND 128 THEN MID$(A$,33,6)="???? ?"
6175 IF (BYTE1B AND 248) = 0 THEN MID$(A$,33,6)=" " 'watch for no data
6180 REM raveling and flushing
6185 IF BYTE2A AND 16 THEN MID$(A$,44,1)="F" ELSE MID$(A$,44,1)="R"
6190 TEMP=BYTE2A AND 3
6195 IF TEMP = 1 THEN MID$(A$,46,2)="S1" ELSE IF TEMP = 2 THEN MID$(A$,46,2)="Mo" ELSE IF TEMP = 3 THEN MID$(A$,46,2)="Se"
6200 TEMP=(BYTE2A\4) AND 3
6205 IF TEMP = 1 THEN MID$(A$,49,3)="Loc" ELSE IF TEMP = 2 THEN MID$(A$,49,4)="W.P." ELSE IF TEMP = 3 THEN MID$(A$,49,3)="Ent"
6210 A14$=" ": A15$=" ": A16$=" ": A17$=" ": A18$=" ": A19$=" ": A20$=" "
6215 IF BYTE2A AND 32 THEN MID$(A$,44,8)="? ? ? ? ?"
6220 IF (BYTE2A AND 63) = 0 THEN MID$(A$,44,8)=" " 'test for no data
6225 IF BYTE2B AND 32 THEN MID$(A$,56,1)="*"
6230 IF BYTE2B AND 128 THEN MID$(A$,61,3)="ACP" ELSE MID$(A$,61,3)="BST"
6235 IF BYTE2A AND 64 THEN MID$(A$,69,1)="1"
6240 IF BYTE2A AND 128 THEN MID$(A$,70,1)="2"
6245 IF BYTE1B AND 1 THEN MID$(A$,71,1)="3"
6250 IF BYTE1B AND 2 THEN MID$(A$,72,1)="4"
6255 IF BYTE1B AND 4 THEN MID$(A$,73,1)="5"
6260 PRINT USING "####";NSAM;A$
6265 PTR=PTR+4: I=I+1
6270 IF I<=20 AND PTR<=(S-3) AND NSAM<NSAMP THEN GOTO 6065
6275 INPUT "enter sam# to see a specific sample, (cr) to continue, -1 to stop";MORE
6280 IF MORE=0 THEN IF NSAM)=NSAMP THEN RETURN ELSE IF PTR<=(S-3) THEN GOTO 6050 ELSE PTR=1: GOTO 6020
6285 IF MORE<0 THEN RETURN
6290 IF MORE>NSAMP THEN PRINT "*** Sample number too high ***":MORE=0:GOTO 6275
6295 NSAM=MORE : MORE=1 'wants to see sample number NSAM
6300 NREC= NSAM\ (S\4) +1 'calculate what record we need to read
6305 I=0
6310 IF NREC = (CURREC - 1) THEN GOTO 6345
6315 I=1
6320 IF NREC = CURREC THEN GOTO 6345
6325 IF NREC < CURREC THEN SPCNT=CURREC-NREC : GOSUB 800
6330 IF NREC > CURREC THEN SPCNT=NREC-CURREC : GOSUB 700
6335 IF SPCNT <> 0 THEN GOSUB 900 : RETURN
6340 CURREC = NREC
6345 PTR= 4*(NSAM-1) - S*(NREC-1) + 1 'align ptr to point into proper spot
6350 IF I = 0 THEN GOTO 6050 ELSE GOTO 6020
6355 PRINT "***Glitch!***": PRINT
6360 RETURN
7000 REM routine to forward space by one "interval", which is NRPERF+1 records
7001 REM long. If the positioning is successful then the summary
7002 REM record will be read and displayed and the current record pointer
7003 REM will be left at NRPERF+2.
7010 IF CURREC < 0 THEN GOSUB 900 :RETURN 'abort if tape position is unknown

```

```

7020 SPCNT = NRPERF + NRPERF + 2 - CURREC
7030 GOSUB 700 'forward space to summary record
7040 IF SPCNT(<)0 THEN RETURN 'abort if unable to position
7050 CA=1 :GOSUB 500 'read summary
7060 IF ECODE = 0 THEN GOTO 7100
7070 IF (DS AND 4) = 0 THEN GOSUB 900: RETURN 'error but not end of track
7080 IF TRACK < 4 THEN TRACK=TRACK+1 : GOTO 7050
7090 GOSUB 900: RETURN 'end of tape, most likely
7100 GOSUB 600 'load into rbuf()
7110 MISPOS = 0 'not mispositioned
7115 HEADSUM$ = "SUM"
7120 GOSUB 3200 'display summary
7130 IF MISPOS=-1 THEN PRINT "***not on summary record***":GOSUB 900: RETURN
7140 CURREC=NRPERF+2
7150 RETURN

8000 REM routine to reverse space by one interval, similar to above
8010 IF CURREC < 0 THEN GOSUB 900:RETURN 'abort if lost
8020 SPCNT = CURREC
8030 GOSUB 800 'reverse space to summary record
8040 IF SPCNT(<)0 THEN RETURN 'abort if unable to position
8050 CA=1 :GOSUB 500 'read summary
8060 IF ECODE = 0 THEN GOTO 8100
8070 IF (DS AND 4) = 0 THEN GOSUB 900: RETURN 'error but not end of track
8080 IF TRACK < 4 THEN TRACK=TRACK+1 : GOTO 8050
8090 GOSUB 900: RETURN 'end of tape, most likely
8100 GOSUB 600 'load into rbuf()
8110 MISPOS = 0 'not mispositioned
8115 HEADSUM$ = "SUM"
8120 GOSUB 3200 'display summary
8130 IF MISPOS=-1 THEN PRINT "***not on summary record***":GOSUB 900: RETURN
8140 CURREC=NRPERF+2
8150 RETURN

9000 REM routine to recompute summary values from raw data in data blocks
9010 F1=0 : F2=0 : F3=0 : F4=0 : F5=0 'flag counters
9020 AC1=0: AC2=0: AC3=0: SAC!=0!: EAC!=0!
9030 LC1=0: LC2=0: LC3=0: SLC!=0!: ELC!=0!
9040 TCN1=0: TCN2=0: TCN3=0: STC!=0!: ETC!=0!
9050 PAA=0: PAB=0: SPA!=0!: EPA!=0!
9060 SRA!=0!: SFL!=0!: ERA!=0!: EFL!=0!
9065 DAC!=0! : DLC!=0! : DTC!=0! : DPA!=0!
9070 IF CURREC < 0 THEN GOSUB 900: RETURN 'abort if lost
9080 SPCNT=CURREC-1 : GOSUB 800 'backspace to start of data
9090 IF SPCNT(<)0 THEN RETURN 'return if unable to position
9095 NEXEMPT = 0 'number of samples with pavement exempt active
9100 FOR I=1 TO NRPERF 'loop on data blocks
9110 CA=1: GOSUB 500 'read data block
9120 IF ECODE = 0 THEN GOTO 9160 'jump if no errors
9130 IF (DS AND 4) = 0 THEN GOTO 9150 'jump if not EOTrack
9140 IF TRACK < 4 THEN TRACK=TRACK+1: GOTO 9110 'try next track
9150 PRINT "***Unexpected filemark error***" : GOSUB 900 : RETURN
9160 PRINT "Tallying block",I,"of",NRPERF,"Please wait."
9170 GOSUB 600 'read data block into rbuf()
9180 FOR PTR=1 TO S STEP 4
9190 BYTE1A=RBUF(PTR)
9200 BYTE1B=RBUF(PTR+1)

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```

9210 BYTE2A=RBUF(PTR+2)
9220 BYTE2B=RBUF(PTR+3)
9225 IF BYTE2B AND 32 THEN NEXEMPT=NEXEMPT+1 : GOTO 9500
9230 REM code to tally up counts of bad road from the four bytes of raw data
9240 IF BYTE1A AND 16 THEN GOTO 9290 'check for bad alligators
9250 IF BYTE1A AND 1 THEN AC1=AC1+1
9260 IF BYTE1A AND 2 THEN AC2=AC2+1
9270 IF BYTE1A AND 4 THEN AC3=AC3+1
9280 IF BYTE1A AND 8 THEN IF BYTE1A AND 4 THEN AC3=AC3+1 ELSE IF BYTE1A AND 2 THEN AC2=AC2+1 ELSE AC1=AC1+1
9290 IF BYTE2B AND 16 THEN GOTO 9340 'check for bad longit cracks
9300 IF BYTE2B AND 1 THEN LC1=LC1+1
9310 IF BYTE2B AND 2 THEN LC2=LC2+1
9320 IF BYTE2B AND 4 THEN LC3=LC3+1
9330 IF BYTE2B AND 8 THEN IF BYTE2B AND 4 THEN LC3=LC3+1 ELSE IF BYTE2B AND 2 THEN LC2=LC2+1 ELSE LC1=LC1+1
9340 IF BYTE1A AND 32 THEN TCN1=TCN1+1
9350 IF BYTE1A AND 64 THEN TCN2=TCN2+1
9360 IF BYTE1A AND 128 THEN TCN3=TCN3+1
9370 IF BYTE1B AND 128 THEN GOTO 9400
9380 TEMP=(BYTE1B\8) AND 7
9390 IF BYTE1B AND 64 THEN PAA=PAA+TEMP ELSE PAB=PAB+TEMP
9400 IF BYTE2A AND 32 THEN GOTO 9450
9410 TEMP=(BYTE2A AND 3)
9420 IF BYTE2A AND 16 THEN SFL!=SFL!+TEMP ELSE SRA!=SRA!+TEMP
9430 TEMP=(BYTE2A\4) AND 3
9440 IF BYTE2A AND 16 THEN EFL!=EFL!+TEMP ELSE ERA!=ERA!+TEMP
9450 IF BYTE2A AND 64 THEN F1=F1+1 'flag counters
9460 IF BYTE2A AND 128 THEN F2=F2+1
9470 IF BYTE1B AND 1 THEN F3=F3+1
9480 IF BYTE1B AND 2 THEN F4=F4+1
9490 IF BYTE1B AND 4 THEN F5=F5+1
9500 NEXT PTR
9510 NEXT I 'tallying done, now compute severities and extents
9520 CA=1: GOSUB 500 'read summary block
9530 IF ECODE = 0 THEN GOTO 9570 'jump if no errors
9540 IF (DS AND 4) = 0 THEN GOTO 9560 'jump if not E0Track
9550 IF TRACK < 4 THEN TRACK=TRACK+1: GOTO 9520 'try next track
9560 PRINT "***Unexpected filemark error***" : GOSUB 900 : RETURN
9570 GOSUB 600 'load data into rbuf()
9580 CURREC = NRPERF+2
9590 N3=256*RBUF(115)+RBUF(116) 'N3, number of samples recorded
9591 NS = N3 - NEXEMPT 'number of unexempted samples
9592 IF NS <= 0 THEN NS = 1
9600 LENGTH!=(256*RBUF(55)+RBUF(56)+(256!RBUF(57)+RBUF(58))/10000!)*5280!
9605 IF (AC1+AC2+AC3)=0 THEN SAC!=0 : EAC!=0 : GOTO 9640
9610 SAC!=(AC1+2*AC2+3*AC3)/(AC1+AC2+AC3)
9620 EAC!=1.5*(AC1+AC2+AC3)/NS + 1!
9630 IF EAC! < 1.04 THEN EAC!=0!: SAC!=0!
9640 IF EAC! > 4! THEN EAC!=4!
9641 DAC! = 5 * (3*SAC! + 2*EAC! - 3)
9642 IF DAC! < 0 THEN DAC! = 0
9645 IF (LC1+LC2+LC3)=0 THEN SLC!=0 : ELC!=0 : GOTO 9670
9650 SLC!=(LC1+2*LC2+3*LC3)/(LC1+LC2+LC3)
9660 ELC!=(LC1+LC2+LC3)/NS + 1!
9670 IF ELC! <= 1.01 THEN ELC!=0! : SLC!=0!
9671 DLC! = 10 * (SLC! + ELC!) - 15

```

```

9672 IF DLC! < 0 THEN DLC! = 0
9675 IF (TCN1+TCN2+TCN3)=0 THEN STC!=0!: ETC!=0!: GOTO 9700
9680 STC!=(TCN1+2*TCN2+3*TCN3)/(TCN1+TCN2+TCN3)
9690 ETC! = .78 + 22*(TCN1+TCN2+TCN3)/LENGTH!
9700 IF ETC! > 3! THEN ETC!=3!
9710 IF ETC! < 1! THEN ETC!=0! :STC!=0!
9711 DTC! = 5 * (STC! + ETC! - 1)
9712 IF DTC! < 0 THEN DTC! = 0
9715 IF (PAA+PAB+F1)=0 THEN SPA!=0 : EPA!=0 : GOTO 9740
9720 SPA!=(PAB +2*PAA + 3*F1)/(PAA+PAB+F1)
9730 EPA!=2!*(PAA+PAB+F1)/NS + 1!
9740 IF EPA! < 1! THEN EPA!=0!: SPA!=0!
9750 IF EPA! > 3! THEN EPA!=3!
9751 DPA! = 10 * (SPA! + EPA! -1)
9752 IF DPA! < 0 THEN DPA! = 0
9760 SRA!=SRA!/NS: SFL!=SFL!/NS: ERA!=ERA!/NS: EFL!=EFL!/NS
9765 IF AUTOSUM=1 THEN RETURN
9770 RECOMP=1:HEADSUM$="SUM": GOSUB 3405: RECOMP=0 'call display routine
9780 RETURN
10000 REM routine to space forward file (sequence)
10010 CA=5: GOSUB 500 'forward space
10020 IF (ECODE=0)AND((DS AND 4)=0)THEN GOTO 10060 'if no errors then jump
10030 IF (DS AND 4) = 0 THEN GOSUB 900: RETURN ' bail out if lost
10040 IF TRACK < 4 THEN TRACK = TRACK+1: GOTO 10010 'step to next track
10050 PRINT "****end of tape!***" :GOSUB 900 :RETURN ' abort on EOTape
10060 MISPOS=0 'should now be at header record
10070 GOSUB 4080 'read and display supposed header record
10080 IF MISPOS = -1 THEN RETURN 'if lost then abort
10090 CURREC=1
10100 RETURN
11000 REM routine to reverse space file (sequence)
11005 I=0
11010 CA=7: GOSUB 500 'reverse space
11020 IF (ECODE=0)AND((DS AND 12)=0) THEN GOTO 11055
11025 IF (DS AND 4)() 0 THEN GOTO 11010 'at extreme end of track (EWS)
11030 IF (DS AND 8) = 0 THEN GOSUB 900: RETURN ' bail out if lost
11040 IF TRACK > 1 THEN TRACK = TRACK-1: GOTO 11010 'step to previous track
11050 PRINT "***beginning of tape!***" :GOTO 11080 'step over space command
11055 IF I=0 THEN I=1 : GOTO 11010
11060 CA=4: GOSUB 500 'step over filemark
11070 MISPOS=0 'should now be at header record
11080 GOSUB 4080 'read and display supposed header record
11090 IF MISPOS = -1 THEN RETURN 'if lost then abort
11100 CURREC=1
11110 RETURN
12000 REM routine to retension tape by running it from one end to the other
12010 TRACK=2
12020 CA=72 'send status bytes relative to BOT
12030 GOSUB 500
12040 TRACK=1
12050 GOSUB 2000 'rewind and read first header record
12060 RETURN
13000 REM routine to do automated summaries of all intervals in a sequence
13010 AUTOSUM=1
13015 GOSUB 4000 'read sequence header

```


DBASE SOFTWARE

```
* EXPAND will take an INTERP input data file, load it
* into dBase and expand all the severity and extent fields
* from one column to two.
accept 'What is the data file name? ' to rdfname
set console off
store at('.',rdfname) -1 to perpos
store substr(rdfname,1,perpos) to stemname
set console on
use narrow
? 'loading data'
append from &rdfname sdf
use wide
copy structure to &stemname
use &stemname
? 'reformatting data'
append from narrow
use narrow
set safety off
zap
set safety on
use &stemname
? rdfname + ' loaded'
```


AVE.PRG

```
* AVE will average severities and extents over a user
* selected length to a new file
accept "Enter the SR - dir - beg mile code " to fstem
set talk off
if type('fstem') <> 'C'
    ? 'File name must be a character expression'
    return
endif
* first open correct files
close databases
select 1
store "H" + fstem to fname
use &fname alias header
select 2
store "D" + fstem to fname
use &fname alias sevext
select sevext
store "A" + fstem to fname
copy structure to &fname
select 3
use &fname alias aved
* determine how many records to average into one
select header
go 1
average int_length next 1 to il
? "Interval length is " + str(il,5,3) + " miles"
input "Enter averaging window length (in miles) " to aveleng
store int(aveleng/il) to nint
? "Averaging " + str(nint,2,0) + " intervals at a time"
*
* NINT is now the number of intervals (number of records in
* SEVEXT) to average over. The AVERAGE function puts its
* results in memory variables which are then REPLACED into a
* new blank record in AVED, the averaged file. One variable,
* the length fraction, is summed rather than averaged so that
* it can be used with the header file to determine the actual
* length of the averaged segments.
*
select sevext
go 1
do while .not.eof()
    currec = recno()
    average next nint to in,od, acs,ace,acd, lcs,lce,lcd, tcs,tce,tcd,
        pas,pae,pad, ras,rae, fls,fle, lf
    go currec
    sum next nint leng_frac to lf
    select aved
    append blank
    replace intno with in,od_reading with od, acsev with acs,
        acext with ace, acded with acd, lcsev with lcs, lcext with lce,
        lcded with lcd, tcsev with tcs, tcext with tce, tcded with tcd
```

```

replace pasev with pas, paext with pae, padded with pad, rasev with ras,
raext with rae, flsev with fls, flex with fle, leng_frac with lf
select sevect
if .not.eof()
go recno()+1
endif
enddo
release in,od, acs,ace,acd, lcs,lce,lcd, tcs,tce,tcd, pas,pae,pad,
ras,rae, fls,fle, lf, aveleng,il,nint,currec
set talk on
? str(recno(),5,0) + " records averaged"

```

LOAD.PRG

```

* This procedure will load the severity and extent and
* header data into dBase files.
set talk off
accept "Enter the State Route - direction - begin mile code, e.g. 123P1 "
accept "Enter the directory, if other than default " to fdir
if len(fdir) > 1
set path to &fdir
endif
close databases
select 1
use header
store "H" + fstem to fname
copy structure to &fname
use &fname alias header
store fname+".DAT" to fname
append from &fname sdf
store "D" + fstem to fname
select 2
use sevect
copy structure to &fname
use &fname alias sevect
store fname + ".DAT" to fname
append from &fname sdf
? "Header and data files loaded"
set talk on

```

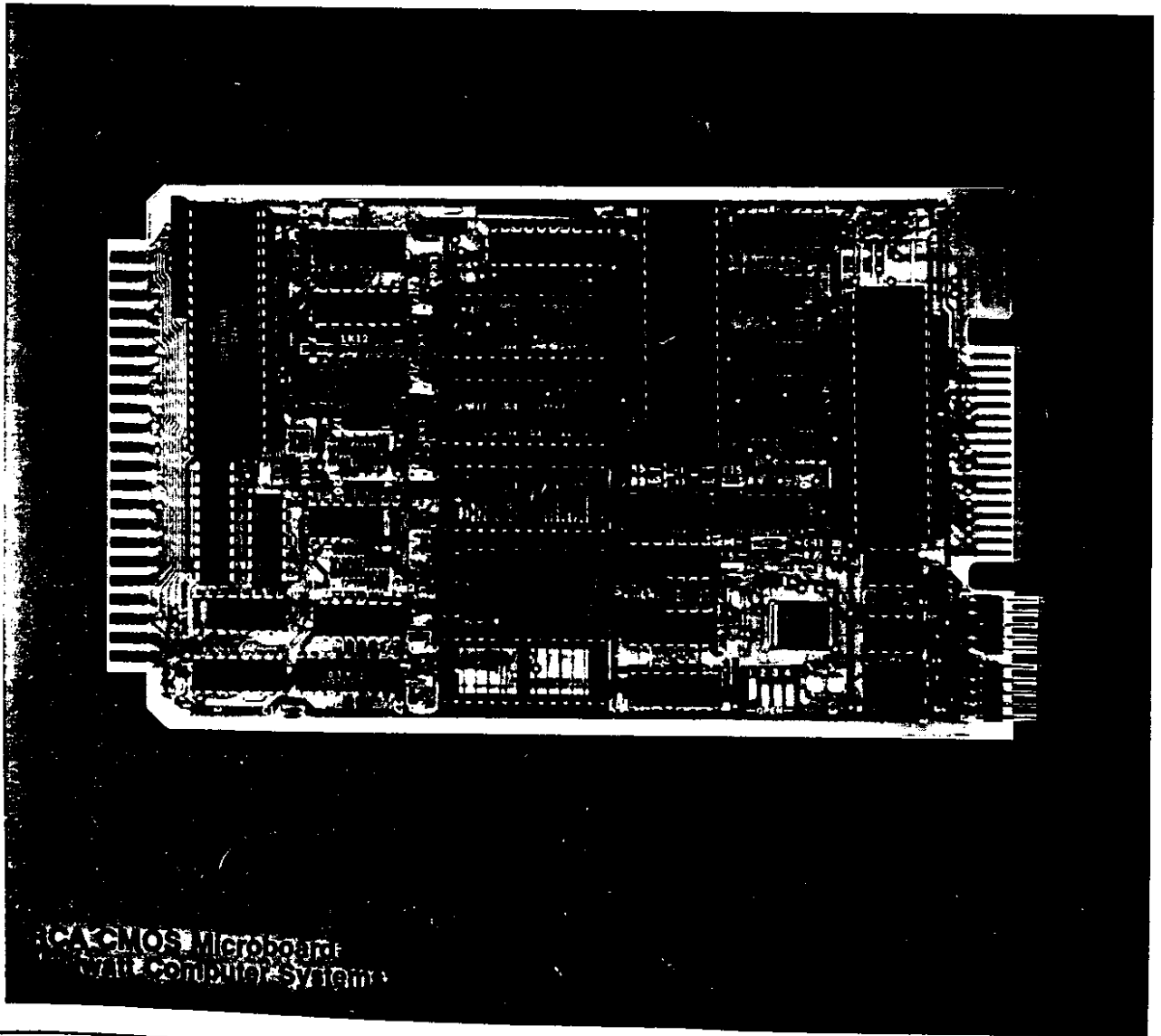
APPENDIX D

HARDWARE MANUALS

RCA Solid
State

RCA CMOS Microboard Computer

CDP18S600



RCA CMOS Microboard
Full Computer System

MB-600

602

RCA CMOS Microboard Computer CDP18S600

The RCA Microboard Computer CDP18S600 is a versatile computer system on a single 4.5 x 7.5 inch card. It features a CDP1805A CPU with a powerful expanded instruction set, and can run at up to twice the speed of previous RCA CPU cards. The card contains a complete UART driven RS232 or RS422 serial data link with handshaking, and more than 20 lines of programmable parallel I/O ports. Five memory sockets are provided, one populated with a 2-K byte RAM, allowing a total mix of RAM, EPROM or ROM of up to 40 kilobytes. A crystal controlled oscillator, power-on clear circuitry, and a full Microboard expansion interface complete the board.

The CDP18S600 is a powerful stand alone system, but it may be combined with any of the broad line of Microboard components for larger applications. (Not all Microboards at present will run at the higher of the 2 selectable clock speeds of the CDP18S600; consult RCA.) The CDP18S600 is plug-in compatible with the RCA MSI series of Industrial Chassis and with the RCA Microboard Computer Development Systems (MCDS) CDP18S693 and CDP18S694 and Color MCDS CDP18S695 to facilitate hardware and software development. It can

Features

- Low power static CMOS — requires 20 mA (typ.)*
 - Operable from a single 5 volt supply
 - High noise immunity
 - 2.46 or 4.92 MHz crystal clock
 - Compatible with RCA MSI series Industrial Chassis and 1800-based development systems
 - Stand alone capability
 - 2 kilobytes of read/write memory — socketed
 - Sockets for up to 40 kilobytes of ROM, EPROM, or byte-wide RAM (including socket above)
 - Power-on reset
 - 1800 series Microprocessor architecture
 - Flexible memory and I/O expansion
 - 20 programmable parallel I/O lines, plus 4 testable flag inputs and Q output
 - 8-bit counter-timer with prescaler
 - UART driven serial I/O
 - RS232, RS422, or CMOS level serial interface
 - 15 selectable BAUD rates: 50 to 38,400
 - Addresses full 64 Kbyte memory space
 - 44 pin system interface
 - Wide temperature range: -40°C to +85°C.
 - Small board size: 4.5 x 7.5 inches
- *with CMOS ROM and CMOS level serial interface

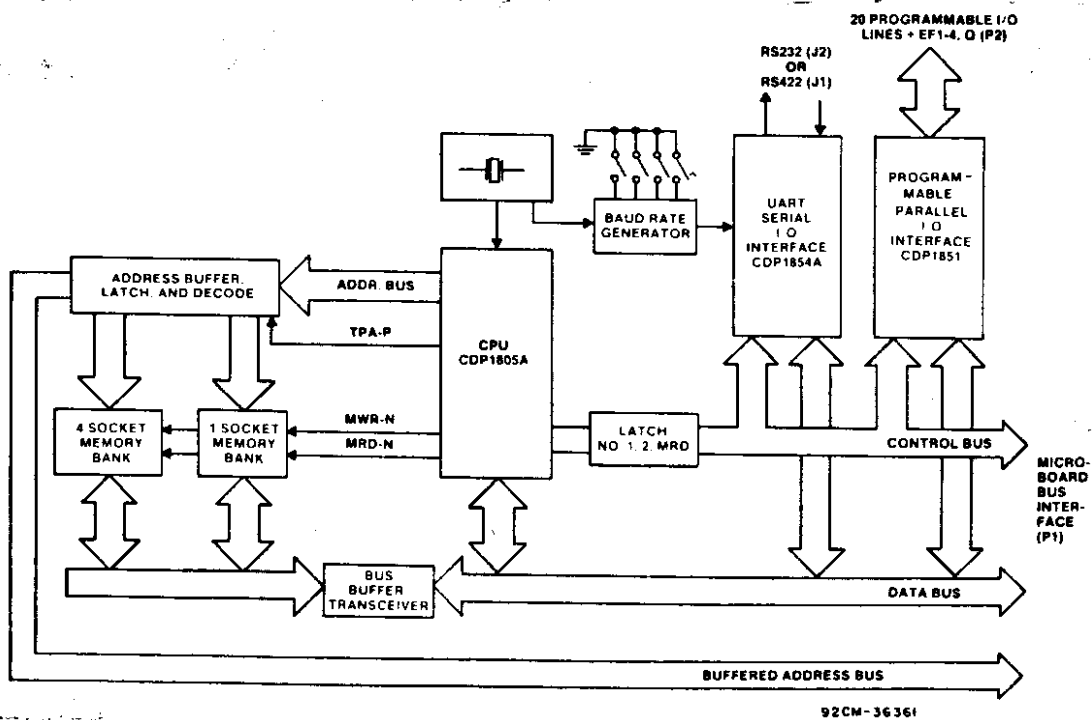


Fig. 1 - Block Diagram of RCA CMOS CDP18S600 Microboard Computer

RCA 1800

MICROSYSTEMS

also be used with the RCA Development System CDP-18S008 (CDSIV) and the MicroDisk Development System (MS2000).

Because of its CMOS design and low current requirements, the power supply and cooling requirements are minimal. A complete system, including an RS422 data link, could run from a small plug in power supply such as the CDP18S023.

Component Features

Central Processing Unit: The central processor for the CDP18S600 is the 8-bit silicon gate CMOS RCA CDP-1805A. The CDP1805A features 16 general purpose 16-bit registers, any of which can be used as program counter, stack or data pointer, or general data storage. One register serves as a program counter for interrupt servicing, while a second can serve as a DMA pointer for fast I/O transfer of data. If either DMA or Interrupt is unused, its register is free for other uses. A versatile 8-bit counter-timer with prescaler, 4 testable flag lines, a single bit testable output port, and several powerful new instructions are also featured.

Memory: The CDP18S600 provides 2 independent banks, one of 4 sockets and one of one. A 6116 CMOS RAM provided in one of the sockets gives 2 Kbytes of read/ write storage. All 5 sockets may be loaded with 2716 (2K x 8), 2732 (4K x 8), or 2764 (8K x 8) compatible EPROM's or masked ROM's, or 6116 (2K x 8) or 6264 (8K x 8) compatible RAM's.

Serial I/O: A serial communications interface, driven by a CDP1854A UART, has EIA RS232 and RS422 capability. The data format is software selectable, while 15 BAUD rates, from 50 to 38,400, are selectable by a 4-position DIP switch.

Parallel I/O: 20 programmable input or output lines are provided by a CDP1851 programmable parallel I/O port. Each line can be customized to an input or output under software control, while several may be used to provide handshaking for byte transfer applications. The CPU flag and Q lines may also be used as input and output respectively.

Specifications

Memory Capacity

On-board ROM/ EPROM/ RAM: 5 sockets for up to 40 kilobytes

On-board RAM: 2 kilobytes occupying one of the above sockets

Off-board expansion: Up to 64 kilobytes total memory space

Memory Address Map

On-board RAM: any 2 kilobyte block

On-board ROM/ EPROM/ RAM: depending on type and quantity of memory, any 2-, 4-, 8-, 16-, or 32-kilobyte block

I/O Capacity

Parallel: 20 lines, each programmable as input or output. 8 of the above are programmable as bidirectional. 4 additional flag inputs and 1 additional bit output.

Serial: Data input and output, and clear to send input and output. Programmable format and switch selectable BAUD rate. RS232, RS422, or CMOS level interface.

Operating Temperature Range

-40°C to +85°C.

Dimensions

4.5 x 7.5 inches (114 x 191 mm)

Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements

(except as noted, 5 volts \pm 10%, @ 2.46 or 4.92 MHz)
Without ROM's or serial interface

6 mA in Reset mode (clock independent)

11 or 13 mA in Wait mode, memory access off-board

15 or 23 mA operating all memory access off-board
47 or 53 mA operating every cycle on-board RAM access

With RS422 driver installed (U3)

55 mA additional

With RS232/ RS422 receiver installed (U2)

35 mA additional

Optional supplies needed for RS232 driver (U4)

+10 to +15 volts at 8 mA typ.

-5 to -15 volts at 8 mA type.

Connectors

System Interface: Double sided edge fingers, 0.156 inch pitch, 44 conductors

Parallel I/O: Double sided edge fingers, 0.100 inch pitch, 34 conductors

Serial I/O: separate RS422 and RS232 10-pin right angle connectors, 2 row, 0.100 inch spacings (mating headers supplied)

Clock

CPU and Interface: 9.8304 MHz crystal controlled oscillator, divided to 4.9152 or 2.4576 MHz

RCA CMOS Microboard Computer CDP18S600

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the CDP18S600 CPU Microboard and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1805A (File No. 1370). For a list of the pins and signals for the RCA Microboard Universal Backplane Connector (P1) as used on the CDP18S600, see Table 1.

DB7 through DB0 — Eight bidirectional data bus lines. Taken directly from the CPU bus pins, these lines transfer data among the memory, CPU, and I/O devices.

N0, N1, N2 — Taken directly from the CPU pins, these lines indicate an I/O instruction is being executed. They are derived from the low-order three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the $\overline{\text{MRD}}$ line. When high, $\overline{\text{MRD}}$ indicates data transfer from I/O to memory; when low, from

memory to I/O.

EF1, EF2, EF3, EF4 — Taken directly to the CPU pins, these inputs can be tested by conditional branch instructions. They, along with INT, DMAI, and DMAO are pulled high (inactive) with resistors. EF1 and EF2, gated by the PIO group address, are used to test the ready state of I/O ports A and B. EF3 and EF4, gated by the UART group address, are used to test the UART interrupt output and the serial data input line. The EF lines may be used to identify the source of an interrupt to the CPU, or they may be used to indicate priority or status.

INT — Taken directly to the CPU pin, the interrupt line causes a transfer of control from the current program counter to register I. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of $\overline{\text{INT}}$ results in completion of execution of the current instruction, followed by an S3 machine state during which designators X and P are stored in T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with RI as program counter.

**Table 1: Pin Terminals and Signals for the
RCA Microboard Universal Backplane**

Component Side				Wire Side			
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
1	DMAI-N	In	DMA Input Request	A	TPA-P	Out	System Timing Pulse 1
2	DMAO-N	In	DMA Output	B	TPB-P	Out	System Timing Pulse 2
3	RNU-P	In	Run Utility Request	C	DB0-P	In/Out	Data Bus
4	INT-N	In	Interrupt Request	D	DB1-P	In/Out	Data Bus
5	MRD-N	Out	Memory Read	E	DB2-P	In/Out	Data Bus
6	Q-P	Out	Programmed Output Latch	F	DB3-P	In/Out	Data Bus
7	SC0-P	Out	State Code	H	DB4-P	In/Out	Data Bus
8	SC1-P	Out	State Code	J	DB5-P	In/Out	Data Bus
9	CLEAR-N	In	Clear-Mode Request	K	DB6-P	In/Out	Data Bus
10	WAIT-N	In	Wait-Mode Request	L	DB7-P	In/Out	Data Bus
11	-5V/-15V	—	Auxiliary Power	M	A0-P	Out	Multiplexed Address Bus
12	SPARE	—	Not Assigned	N	A1-P	Out	Multiplexed Address Bus
13	CLOCK OUT	Out	Clock from CPU Osc.	P	A2-P	Out	Multiplexed Address Bus
14	N0-P	Out	I/O Primary Address	R	A3-P	Out	Multiplexed Address Bus
15	N1-P	Out	I/O Primary Address	S	A4-P	Out	Multiplexed Address Bus
16	N2-P	Out	I/O Primary Address	T	A5-P	Out	Multiplexed Address Bus
17	EF1-N	In	External Flag	U	A6-P	Out	Multiplexed Address Bus
18	EF2-N	In	External Flag	V	A7-P	Out	Multiplexed Address Bus
19	EF3-N	In	External Flag	W	MWR-N	Out	Memory Write Pulse
20	+10V/+15V	—	Auxiliary Power	X	EF4-N	In	External Flag
21	+5V	—	+5 V dc	Y	+5V	—	+5V dc
22	GND	—	Digital Ground	Z	GND	—	Digital Ground

Note: Signal flow direction is relative to CPU.

RCA 1800

MICROSYSTEMS

Interrupts can result from an external source or from the counter timer. Each can be separately enabled with XIE or CIE instructions

DMAI, DMAO — Taken directly to CPU pins and not utilized by the CDPI8S600, these lines allow off-board I/O controllers rapid direct memory access. The CPU monitors these data transfers, going into an S2 machine state for each byte transfer. R0 is used as the memory pointer and is automatically incremented each time. Thus, DMA transfers are interleaved with normal processing and no software action is required except to initialize R0 before transfer starts. INT and or an EF may be used to notify the program that a block DMA transfer is completed so that initialization and processing of the data block may be performed. The DMA inputs may be maintained in the true state for contiguous S2 states for the most rapid transfer. In the usual case, however, the DMA request is removed at the TPA of the S2 cycle to obtain a single byte transfer, allowing time for normal processing and for setting up the next byte in the requesting controller. Each S2 state is eight clock cycles in duration.

SC1, SC0 — State code outputs from the CPU which identify the type of machine cycle in progress.

State Type	State Code Lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

TPA, TPB — Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

All I/O cycles should be considered to start at the trailing edge of TPA and end at the trailing edge of TPB. MRD, the N lines, and the A7 through A0 lines are stable during this period. (To provide additional hold time on these lines, the CDPI8S600 board latches them at TPB trailing edge, and holds them through the next leading edge of TPA.)

A7 through A0 — Eight memory address lines from the CPU. The 16 memory address bits are multiplexed on this address bus. The high-order eight bits are presented early in each machine cycle and must be latched at the TPA trailing edge. The CDPI8S600 buffers, latches,

and decodes these bits for the on-board memories. Any external memory must provide its own latches. During the latter part of the cycle, the low-order eight bits are presented on this address bus and need not be latched.

MWR — A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

MRD — A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. MRD must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of MWR must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while MRD is false before MWR appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures.

Q — A single bit output from the CPU. This bit is set or reset by SEQ (7B) or REQ (7A) instructions, and is also reset by CLEAR. It is available both on the Micro-board Bus (P1) and on the Parallel I/O connector (P2). Q may also be tested with a branch instruction, or may be toggled from the Counter/Timer.

CLOCK OUT — A 4.9152 or 2.4576 MHz square wave clock provided for general use. It is derived from the 9.8304 MHz on-board crystal controlled oscillator.

WAIT, CLEAR — Two control inputs to the CPU which determine the mode of operation.

CLEAR	WAIT	MODE
L	L	Not allowed
L	H	Reset
H	L	Pause
H	H	Run

The functions of the modes are defined as follows:

RESET: Registers I, N, Q, counter prescaler, and counter interrupt (CI) are reset. IE, XIE, and CIE are set and 0's (Vss) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The state of the counter/timer is unaffected by the RESET operation.

The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1, X, P→T, and then registers X, P, and R(0) are reset. Interrupt and DMA

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servicing are suppressed during the initialization cycle. The next cycle is an S0 or an S2 but never an S1 or S3. In most cases, it is desirable to reset the IE before starting processing. The use of a 71 instruction followed by 00 at memory locations 0000 and 0001 will reset IE which may be set later when the software is able to process interrupt. Power-up reset-run is provided on the CDP18S600 board.

PAUSE: Stops the internal CPU timing generator, freezing the state of the processor. Pause can occur at two points in a machine cycle, on the low-to-high transition of either TPA or TPB. The oscillator continues to run but subsequent clock transitions are ignored (see Fig. 2).

If Pause is entered while in the event counter mode, the appropriate E Flag transitions will continue to decrement the counter.

RUN: May be initiated from the Pause or Reset mode functions. If initiated from Pause, the CPU resumes operation at the point it left off. If paused at TPA, it will resume on the first high-to-low clock transition. If paused at TPB, it will resume on the first low-to-high clock transition (see Fig. 2). When run is initiated from the Reset operation, the first machine cycle following Reset is always the initialization cycle.

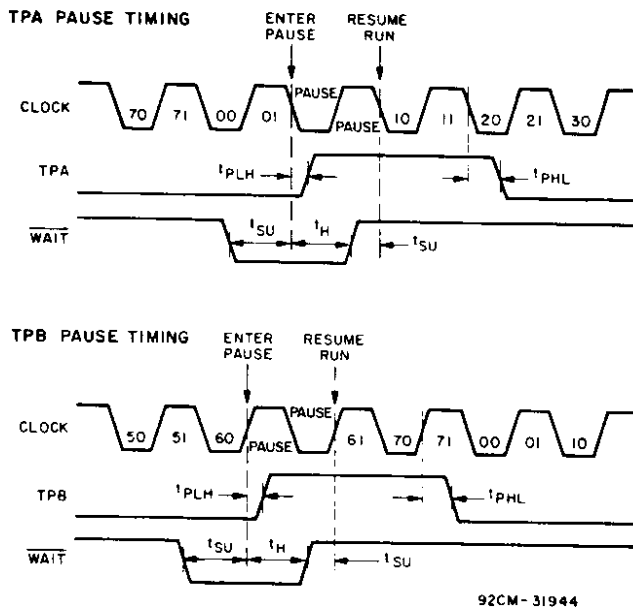


Fig. 2 - Pause mode timing waveforms.

The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

RNU — Run Utility Software. A signal supplied to CDP18S600 to force the most significant address true. As a result, the program start is at memory location 8000 instead of 0000. See discussion under Run Utility.

Counter-Timer and Controls

The CDP1805A provides an on-chip 8-bit presetable timer-counter. Software control of the counter allows the clock input to be $TPA \div 32$, EF1, EF2, $TPA \cdot EF1$, or $TPA \cdot EF2$, in addition to the Decrement-Counter Instruction.

The counter-timer logic shown in Fig. 3 consists of a presetable 8-bit down-counter (Modulo N type), and a conditional divide-by-32 prescaler. After counting down to $(01)_{16}$ the counter returns to its initial value at the next count and sets the Timer/Counter Interrupt. It will continue decrementing on subsequent counts. If the counter is preset to $(00)_{16}$ a full 256 counts will occur.

During a Load Counter instruction (LDC) if the counter was stopped with a STPC instruction, the counter and its holding register (CH) are loaded with the value in the D register and any previous counter interrupt is cleared. If the LDC is executed when the counter is running, the contents of the D register are loaded into the holding register (CH) only and any previous counter interrupt is not cleared. After counting down to $(01)_{16}$ the next count will load the new initial value into the counter, set the Counter Interrupt Latch, and operation will continue.

The timer/counter has the following five programmable modes:

- Event Counter 1:** Input to counter is connected to the $\overline{EF1}$ terminal. The high-to-low transition decrements the counter.
- Event Counter 2:** Input to counter is connected to the $\overline{EF2}$ terminal. The high-to-low transition decrements the counter.
- Timer:** Input to counter is from the divide-by-32 prescaler clocked by TPA. The prescaler is decremented on the low-to-high transition of TPA. The divide-by-32 prescaler is reset when the counter is in a mode other than the Timer mode or stopped by a STPC.
- Pulse Duration Measurement 1:** Input to counter connected to TPA. Each low-to-high transition of TPA decrements the counter if the input signal at $\overline{EF1}$ terminal (gate input) is low. On the transition of $\overline{EF1}$ to the positive state, the count is stopped, the mode is cleared, and the interrupt request latched. If the counter underflows while the input is low, interrupt will also be set, but counting will continue.

5. Pulse Duration Measurement 2: Operation is identical to Pulse Duration Measurement 1, except $\overline{EF2}$ is used as the gate input.

The modes can be changed without affecting the stored count.

Those modes which use $\overline{EF1}$ and $\overline{EF2}$ terminals as inputs do not exclude testing these flags for branch instructions.

The **Stop Counter (STPC)** instruction clears the counter mode and stops counting. The STPC instruction should be executed prior to a GEC instruction, if the counter is in the Event Counter Mode 1 or 2.

In addition to the five programmable modes, the **Decrement Counter instruction (DTC)** enables the user to count in software. In order to avoid conflict with counting done in the other modes, the instruction should be used only after the mode has been cleared by a Stop Counter instruction.

The **Enable Toggle Q instruction (ETQ)** connects the Q-line flip-flop to the output of the counter, such that each time the counter decrements from 01 to its next value, the Q output changes state. This action is independent of the counter mode and the Interrupt Enable flip-flops. The Enable Toggle Q condition is cleared by an LDC with the timer/counter stopped, system Reset, or a BCI with C1=1.

On-Board Memory Addressing

All 1800 series processors use a multiplexed address bus: the high byte is output first to be latched with TPA trailing edge, then the low byte is output. The CDP18S600 also latches the low byte and holds it through the next TPA leading edge. This gives more address hold time after the memory write pulse and TPB. (TPB trailing edge is often used to strobe I/O output data.)

The latched A0 through A10 are sent to each memory socket, while A13 through A15 are decoded for chip selects. A11 and A12 may be used either at the socket or for chip select decoding depending on memory size.

The CDP18S600 provides 2 independent memory "banks", one of 4 sockets and one of 1 socket. Each socket may contain ROM, EPROM, or RAM of 2K x 8, 4K x 8, or 8K x 8 size, the only restriction being that all the memories within one bank be the same size. In addition, each socket may be disabled entirely.

Note that in the following discussion of memory address setting, all links within a given link pack not specifically called out as closed must be removed. Permanent circuit damage could result otherwise. Refer to the Parts List for manufacturers' part no's for Links.

Selecting Memory Type

Each socket, U17 through U21, has an associated 6

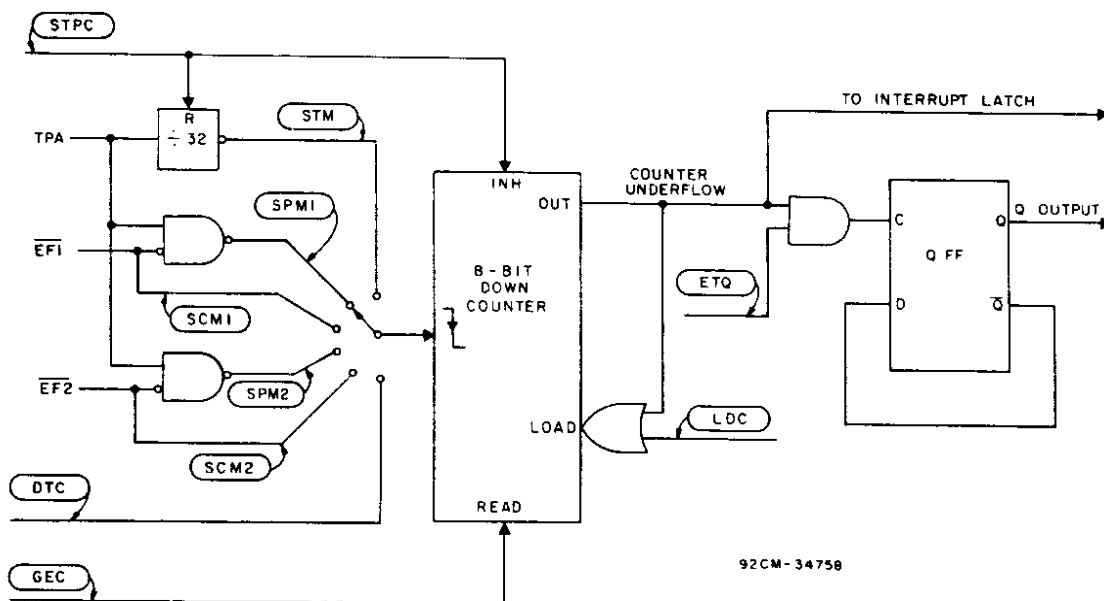


Fig. 3 - Timer/Counter diagram for CDP1805AC and CDP1806AC.

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pin link pack, LK 6 through LK 10, used to set memory type. The link pack is found near pin 28 of each socket; see figure 4 for socket and link placement. Table II lists link connections needed for each memory type.

Table II: Links for setting memory type.

Generic Type	Size	Link
6116 RAM	2K x 8	1 - 2
6264 RAM	8K x 8	1 - 6, 2 - 3
2716 EPROM	2K x 8	2 - 5
2732 EPROM	4K x 8	2 - 3
2764 EPROM	8K x 8	2 - 3, 5 - 6

Note that EPROM's are Intel compatible pinout. Compatible ROM's could be substituted. Note also that a larger memory could be used to fill a smaller "hole," such as using a 6264 as a 4K RAM. Link the socket to fit the memory used, but link the decoder to provide the memory size desired as discussed below.

Note that all memory sockets are 28 pin. When using 24 pin memories, insert the chip so that pins 1, 2, 27, and 28 of the socket are left vacant. The chip should still be facing the same way as the socket.

Setting memory addresses: 1 socket memory bank (U21).

Link packs 11 and 14 (see Fig. 4) set the address of U21. Tables III, IV, and V give link pack 11 and 14 positions for 2K, 4K, and 8K x 8 memory sizes respectively.

Setting memory addresses: 4 socket memory bank (U20, 19, 18, 17).

Link pack 13 (see Fig. 3) sets the addresses of U20, 19, 18, and 17. Tables VI, VII, and VIII give link pack 13 positions for 2K, 4K, and 8K x 8 memory sizes respectively. Note that all link pack 12 links should also be made except when it is desired to disable a socket as discussed below.

Disabling memory sockets

As memory data lines are buffered, simply removing a memory chip will not free up that memory space. See Table IX for disabling each memory socket. As previously mentioned, link packs 6 through 10 are located near pin 28 of sockets U17 through 21.

To avoid floating inputs on the memory decoders, unused memory banks must still have a valid address setup on link packs 13 or 14.

When a socket is disabled, remove the contained memory chip.

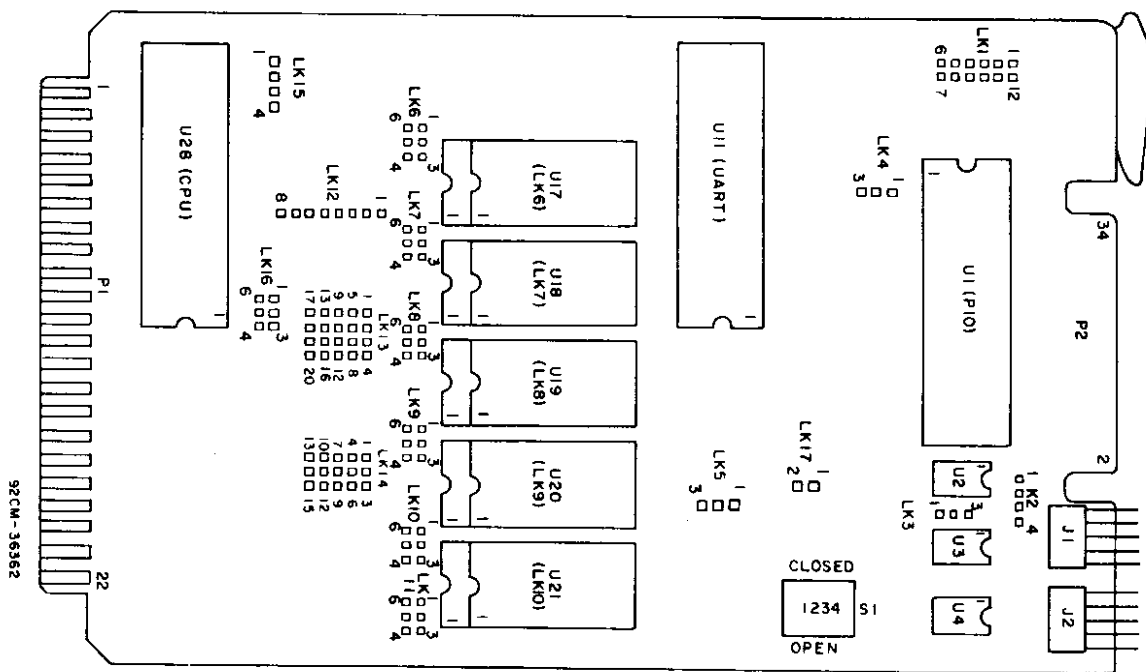


Fig. 4 - Links, Connectors, Baud Rate Switch, and Socketed I.C.s.

Table III: I Socket Memory Bank (U21) Linking for 2Kx8 Memory Chips

MEMORY ADDRESS		LK11			
	LK14				
		5 - 6	1 - 2	2 - 3	4 - 5
2 - 3, 5 - 6	7 - 8, 10 - 11, 13 - 14	0000 - 07FF	0800 - 0FFF	1000 - 17FF	1800 - 1FFF
	8 - 9, 10 - 11, 13 - 14	2000 - 27FF	2800 - 2FFF	3000 - 37FF	3800 - 3FFF
	7 - 8, 11 - 12, 13 - 14	4000 - 47FF	4800 - 4FFF	5000 - 57FF	5800 - 5FFF
	8 - 9, 11 - 12, 13 - 14	6000 - 67FF	6800 - 6FFF	7000 - 77FF	7800 - 7FFF
	7 - 8, 10 - 11, 14 - 15	8000 - 87FF	8800 - 8FFF	9000 - 97FF	9800 - 9FFF
	8 - 9, 10 - 11, 14 - 15	A000 - A7FF	A800 - AFFF	B000 - B7FF	B800 - BFFF
	7 - 8, 11 - 12, 14 - 15	C000 - C7FF	C800 - CFFF	D000 - D7FF	D800 - DFFF
	8 - 9, 11 - 12, 14 - 15	E000 - E7FF	E800 - EFFF	F000 - F7FF	F800 - FFFF

**Table IV: I Socket Memory Bank (U21)
Linking for 4Kx8 Memory Chips**

Memory Address		LK11	
	LK14		
		5 - 6	2 - 3
1 - 2, 5 - 6	7 - 8, 10 - 11, 13 - 14	0000 - 0FFF	1000 - 1FFF
	8 - 9, 10 - 11, 13 - 14	2000 - 2FFF	3000 - 3FFF
	7 - 8, 11 - 12, 13 - 14	4000 - 4FFF	5000 - 5FFF
	8 - 9, 11 - 12, 13 - 14	6000 - 6FFF	7000 - 7FFF
	7 - 8, 10 - 11, 14 - 15	8000 - 8FFF	9000 - 9FFF
	8 - 9, 10 - 11, 14 - 15	A000 - AFFF	B000 - BFFF
	7 - 8, 11 - 12, 14 - 15	C000 - CFFF	D000 - DFFF
	8 - 9, 11 - 12, 14 - 15	E000 - EFFF	F000 - FFFF

**Table V: I Socket Memory Bank (U21)
Linking for 8Kx8 Memory Chips**

Memory Address		LK11
	LK14	
		5 - 6
1 - 2, 4 - 5	7 - 8, 10 - 11, 13 - 14	0000 - 1FFF
	8 - 9, 10 - 11, 13 - 14	2000 - 3FFF
	7 - 8, 11 - 12, 13 - 14	4000 - 5FFF
	8 - 9, 11 - 12, 13 - 14	6000 - 7FFF
	7 - 8, 10 - 11, 14 - 15	8000 - 9FFF
	8 - 9, 10 - 11, 14 - 15	A000 - BFFF
	7 - 8, 11 - 12, 14 - 15	C000 - DFFF
	8 - 9, 11 - 12, 14 - 15	E000 - FFFF

Table VI: 4 Socket Memory Bank (U17 - 20) Linking for 2Kx8 Memory Chips

Memory Address		Memory Socket			
	LK13				
		U20	U19	U18	U17
1 - 2, 6 - 7	10 - 11, 14 - 15, 18 - 19	0000 - 07FF	0800 - 0FFF	1000 - 17FF	1800 - 1FFF
	11 - 12, 14 - 15, 18 - 19	2000 - 27FF	2800 - 2FFF	3000 - 37FF	3800 - 3FFF
	10 - 11, 15 - 16, 18 - 19	4000 - 47FF	4800 - 4FFF	5000 - 57FF	5800 - 5FFF
	11 - 12, 15 - 16, 18 - 19	6000 - 67FF	6800 - 6FFF	7000 - 77FF	7800 - 7FFF
	10 - 11, 14 - 15, 19 - 20	8000 - 87FF	8800 - 8FFF	9000 - 97FF	9800 - 9FFF
	11 - 12, 14 - 15, 19 - 20	A000 - A7FF	A800 - AFFF	B000 - B7FF	B800 - BFFF
	10 - 11, 15 - 16, 19 - 20	C000 - C7FF	C800 - CFFF	D000 - D7FF	D800 - DFFF
	11 - 12, 15 - 16, 19 - 20	E000 - E7FF	E800 - EFFF	F000 - F7FF	F800 - FFFF

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Table VII: 4 Socket Memory Bank (U17 - 20) Linking for 4Kx8 Memory Chips

Memory Address		Memory Socket			
LK13		U20	U19	U18	U17
2 - 6, 3 - 7, 5 - 9	14 - 15, 18 - 19	0000 - 0FFF	1000 - 1FFF	2000 - 2FFF	3000 - 3FFF
	15 - 16, 18 - 19	4000 - 4FFF	5000 - 5FFF	6000 - 6FFF	7000 - 7FFF
	14 - 15, 19 - 20	8000 - 8FFF	9000 - 9FFF	A000 - AFFF	B000 - BFFF
	15 - 16, 19 - 20	C000 - CFFF	D000 - DFFF	E000 - EFFF	F000 - FFFF

Table VIII: 4 Socket Memory Bank (U17 - 20) Linking for 8Kx8 Memory Chips

Memory Address		Memory Socket			
LK13		U20	U19	U18	U17
2 - 3, 7 - 8, 5 - 9, 13 - 17	18 - 19	0000 - 1FFF	2000 - 3FFF	4000 - 5FFF	6000 - 7FFF
	19 - 20	8000 - 9FFF	A000 - BFFF	C000 - DFFF	E000 - FFFF

Table IX: Disabling memory sockets

Disabled socket	Remove links	Add links
U21	LK 10 and LK 11: all	LK 10: 4 - 5
U20	LK 9: all, LK 12: 1 - 2	LK 9: 4 - 5
U19	LK 8: all, LK 12: 3 - 4	LK 8: 4 - 5
U18	LK 7: all, LK 12: 5 - 6	LK 7: 4 - 5
U17	LK 6: all, LK 12: 7 - 8	LK 6: 4 - 5

UART group address; see figure 4 for location. Table X gives the group select choices. Note that utility programs such as UT70 require the UART to be in group 1.

Table X: UART and PIO group addresses

LK4 links	Group	Binary Address
1 - 2	UART group 1	XXXX 0001
2 - 3	UART group 2	XXXX 0010
XXXXX	PIO group 8	XXXX 1000

Note: X = don't care

Serial I/O

The CDP1854A UART has 4 registers. Once the UART group has been enabled, the registers are addressable as in Table XI below.

Table XI: UART I/O register addresses

Out 2: Load transmitter holding register
Out 3: Load control register
Inp 2: Read receiver holding register
Inp 3: Read status register

The control register sets, among other things, the word length, even odd parity, parity enable, and number of stop bits. RCA utility routines, such as contained in RCA Monitor Program CDP18SUT70, set conditions of no parity, 8 data bits, and 2 stop bits. This setup requires an Out 3 instruction with data of hex 1D. For more information on setting up the UART, refer to the data

Input/Output Interfacing

2 Level Addressing

In order to expand the number of I/O addresses available on RCA CDP1800 series microprocessors, a 2 level addressing scheme has been adopted on RCA Microboards. The data output during an "OUT 1" (61) instruction is latched by all I/O type Microboards. (This is referred to as a group select or 2 level address.) Boards decode either the lower nibble (bits 0 - 3) in a linear (1 of 4) manner, or the upper nibble in a binary (1 of 16) manner. Each I/O board compares this group number to the number assigned to it, and if the group matches, it can then respond to subsequent output (62 - 67) or input (6A - 6F) instructions. ("INP 1" (69) is reserved to read back, where implemented, the last group select address. The CDP18S600 board does not provide this function.)

Both the serial I/O, a CDP1854A UART, and the parallel I/O, a CDP1851 PIO, are enabled by linear group select bits. The UART may occupy either group 1 or 2, while the PIO is fixed in group 8. LK4 sets the

sheet for the CDP1854A, file number 1193.

The status register (Inp 3) holds transmitter and receiver status information. When bit 7, transmitter holding register empty, is set, it indicates that it is okay to load another output character for transmission. When bit 0, data available, is set, it indicates that a full character has been received and may be read.

The Out 2 instruction outputs data to be transmitted, and the Inp 2 instruction reads data that has been received.

The UART has an interrupt output that can be programmed to respond to several different status conditions; again refer to file 1193. The interrupt signal can be presented to the CPU INT — N or EF3 — N lines through links on LK1. The SDI (serial data in) signal can be sampled on EF4 — N through a third link on LK1; this allows a break condition to be detected (EF4 False). This link must be in place for running MICRO-DOS or equivalent. See Table XII for LK1 connections and Fig. 4 for LK1 location.

Both EF lines are driven through open collector gates and are disabled by removing the UART group select. The INT line is also open collector, but is not controlled with group select. In a system with multiple interrupts, the source of an interrupt could be determined by enabling group selects until an active flag was found.

Table XII: LK1 Connections

LK1 link	Connects
1 - 12	PIO interrupts to INT — N
2 - 11	UART interrupt to INT — N
3 - 10	PIO ARDY line to EF1 — N
4 - 9	PIO BRDY line to EF2 — N
5 - 8	UART interrupt to EF3 — N
6 - 7	UART SDI line to EF4 — N

The UART circuitry provides clear to send (CTS) handshaking as well as serial data input and output (SDI and SDO). Transmitting is stopped if the external CTS input is low (high at the UART). When receiving, the CTS output is lowered in the middle of the first stop bit, and raised again approximately 1/2 of a bit time after the receiver holding register is read. This allows synchronization of sender and receiver. See Table XIII to disable CTS input handshaking. If U2 has been removed, jumper its socket, pins 2 to 4.

Table XIII: Selecting Serial Interface

Interface	LK2 (CTS)	LK3 (SDI)
RS232	1 - 2	1 - 2
RS422, unterminated	none	none
RS422, terminated with 200 Ohms	3 - 4	3 - 4
Disable (CTS input only)	1 - 2, 3 - 4	—

The serial data and CTS lines may use RS232, RS422, or 0 - 5 volt CMOS signal levels. RS232 uses ± 5 to ± 15 volt single ended signals, while RS422 uses differential 2 volt signal levels. RS422 is intended for transmitting over longer distances or at greater speeds. Note that in RS232 the data is inverted and CTS is active high.

J2 provides the RS232 interface connections; see Table XIV for pin functions, and Fig. 5 for pin placement. U4 is the RS232 driver, and requires auxiliary supplies as outlined in the specifications. For applications where 0 to 5 volt output levels are acceptable, U4 may be removed and pins 1 to 3 and 5 to 7 jumpered. U2 is both the RS232 and RS422 receiver; select interface type by linking LK2 and LK3 as per Table XIII. RS232 and RS422 interfaces cannot be hooked up simultaneously.

J1 provides the RS422 interface. U3 is the RS422 driver while again U2 serves as the receiver. Input signals can be terminated with 200 Ohms to provide matching for longer distance cable runs; see Table XIII. Also see Table XIII to disable CTS input handshaking. When connecting RS422 inputs, the corresponding LK2 or LK3 pin 1 to 2 jumper must be removed; the short could damage the driver.

Table XIV: J1 (RS422) And J2 (RS232) Pin Functions

Pin No.	J1	J2
1	- CTS Out	Ground
2	- Data Out	- Data In
3	KEY	- Data Out
4	- CTS In	Tied High
5	- Data In	KEY
6	+ Data In	Tied High
7	+ CTS In	+ CTS Out
8	Ground	Tied High
9	+ Data Out	+ CTS In
10	+ CTS Out	Ground

J1 also provides a CMOS level interface. This allows a

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low power serial communications link, but with less noise immunity than either RS232 or RS422. Remove U2, U3, and U4. Using 0.3 inch jumpers, connect U2 socket pins 2 to 7 and 3 to 6, and U3 socket pins 2 to 7 and 3 to 6. Open all LK2 and LK3 pins. The former RS422 "+" signal pins now carry the interface, although CTS is active low. If CTS input handshaking is not desired, jumper U2 socket pins 2 to 4.

SW1 sets the BAUD rate over a range of 50 to 38,400

bits/second. See Table XV for a list of available BAUD rates and switch settings.

Parallel I/O

The parallel I/O interface (P2) consists of 20 lines from a CDP1851 programmable I/O port, the CPU Q output and 4 flag inputs, clear, all 3 system supplies, and ground. P2 mates with a 34 conductor, 0.100 inch pitch, card edge connector. (Not supplied; see parts list for appropriate connectors.) See Fig. 5 for orientation, and Table XVI for a list of pin functions.

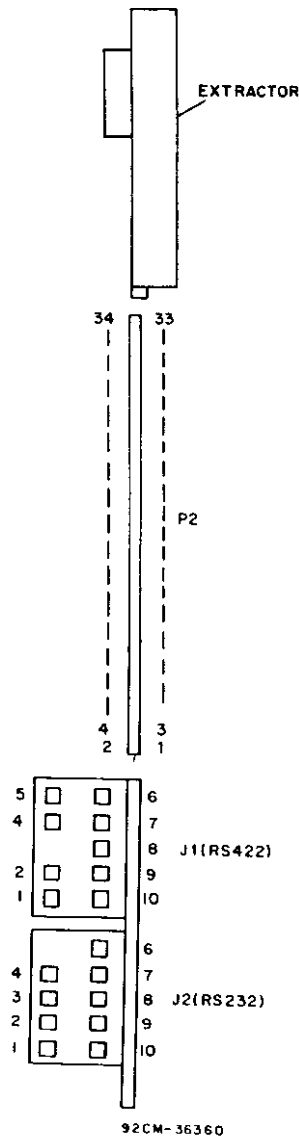


Fig. 5 - I/O Pin Positions - Edge View

Table XV: Baud Rate Selection Chart

Switch S1				Output Rate Baud*
4	3	2	1	
C	C	C	C	19200
C	C	C	O	38400
C	C	O	C	50
C	C	O	O	75
C	O	C	C	134.5
C	O	C	O	200
C	O	O	C	600
C	O	O	O	2400
O	C	C	C	9600
O	C	C	O	4800
O	C	O	C	1800
O	C	O	O	1200
O	O	C	C	2400
O	O	C	O	300
O	O	O	C	150
O	O	O	O	110

*Actual input to UART is 16 times the indicated output rate.

O=Open; C=Closed.

The RCA CDP1851 PIO consists of 2 - 8-bit ports, each with 2 handshaking lines, as well as internal control and status registers. The external ports (A and B) can be programmed as input or output, or one or both can be set in the bit-programmable mode. In this mode, each data and handshake line is a direction-programmable I/O line, and the PIO can generate interrupts on logical combinations of the data lines. Port A can also be placed in a bi-directional mode using all 4 handshake lines (requires port B to be in bit-programmable mode). Ports can be read back in the output mode, allowing a check of last byte output.

After first enabling the PIO group select as discussed previously, the CDP1851 registers may be addressed as in Table XVII. Note that the RCA Monitor Program

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Table XVI: Microboard Computer Parallel I/O Connector (P2)

Pin	Signal	Pin	Signal
1	B2-P	2	GND
3	B1-P	4	B3-P
5	B0-P	6	B4-P
7	BSTB-P	8	B5-P
9	BRDY-P	10	B6-P
11	AD7-P	12	B7-P
13	AD6-P	14	GND
15	AD5-P	16	CLEAR-N
17	AD4-P	18	GND
19	AD3-P	20	Q-P
21	AD2-P	22	GND
23	AD1-P	24	EF4-N
25	AD0-P	26	EF3-N
27	ASTB-P	28	GND
29	ARDY-P	30	+ 5V
31	EF2-N	32	-5V/-15V
33	EF1-N	34	+10V/+15V

CDP18SUT70 also uses group 8 for enabling the CDP-18S651 floppy disk controller. The addresses within the group do not overlap, however, so this board may be operated with the CDP18SUT70 and the CDP18S651. (Software written to run on previous CPU cards such as the CDP18S601 will require shuffling of the PIO addresses.)

Table XVII: CDP1851 I/O Functions

I/O Instruction	CDP1851 Function
OUT 2 (62)	Write to port B
OUT 3 (63)	Write to port A
OUT 6 (66)	Write to Control Register
INP 2 (6A)	Read port B
INP 3 (6B)	Read port A
INP 6 (6E)	Read Status Register

Two of the handshake lines, ARDY and BRDY, can be linked to EF1 and EF2 respectively through open collector drivers. These are enabled with the PIO group select, and present active (low) flags if ARDY or BRDY are low. The two open collector interrupt lines from the PIO are tied together and may be linked to the CPU interrupt line. These are not conditioned with group select. Table XII gives linking. The use of the handshake and interrupt lines will be discussed under each mode of operation.

Setting Modes: The different modes of the PIO can be set by doing an OUT 6 with the data contained in Table XVIII. Note that modes should be set in the order shown; don't set port B as bit programmable then try to set port A as output. Also note that only port A can be bidirectional, and if set so, port B has to be bit programmable.

Table XVIII: Mode set and interrupt enable control words (OUT 6)

	PORT A	PORT B	BOTH PORTS
Input	0B	13	1B
Output	4B	53	5B
Bit-Programmable	CB*	D3*	DB*
Bi-Directional	8D	—	—
Enable Interrupts	81	89	—
Disable Interrupts	01	09	—

*Note: When Bit-Programmable mode is set, a second OUT 6 must follow with data to set bit direction: see text.

Enabling Interrupts: In the following mode discussions, interrupts can be used for a variety of handshaking chores or can result from a programmable logical function of input or output bits. To enable or disable interrupts, the data contained in Table XVIII must be written to the control register (OUT 6). This shouldn't be done until all other setup is accomplished. Reset disables all interrupts. Note that when interrupts are disabled, neither the open collector interrupt drivers nor the interrupt bits in the status register can be active.

Input Mode: The input mode is entered either from reset or by setting it as in Table XVIII. If ASTB or BSTB is high (pulled high by on-board 10 KOhm resistors), then input data can be read continuously. If handshaking is desired, strobing ASTB or BSTB high then low will latch data into port A or B. The leading edge of the strobe will knock down ARDY or BRDY; these signals can then be used to signify "not ready for more data." The trailing edge of the strobe will set the PIO interrupt, if enabled, signalling the CPU to read the data. The leading edge of reading the PIO (INP 3 for port A, INP 2 for port B) will drop the interrupt request from that port, and the trailing edge will set ARDY or BRDY high again.

Since A and B interrupt drivers are tied together, the source must be determined by reading the status register (INP 6 — see Table XIX) or EF1 or 2. Status register bit

RCA CMOS Microboard Computer CDP18S600

1 set or EF1 active indicates port A, while bit 0 or EF2 indicates port B. In a non-interrupt driven system, the status bits alone can be used for determining when data is available. Avoid using the flag lines alone unless the strobe pulse is known to be very narrow.

Note that on first entering the input mode, the ARDY and BRDY lines may be low; doing a "dummy" read will set them high. Also note that the STB, RDY, and all data lines have 10 KOhm pullup resistors.

Output Mode: When data is loaded into ports A or B (OUT 3 or 2), the ARDY or BRDY lines go high signifying "data available." The PIO interrupt goes inactive (if the other port isn't interrupting) as well as the EF1 or EF2 line. An external device accepting the data should respond by strobing ASTB or BSTB high then low. The strobe leading edge will knock down the ARDY or BRDY lines (EF1 or 2 go inactive), and the trailing edge will set the interrupt request. This signifies "data accepted, ready for more." (Output data can be read back if ASTB or BSTB is high.)

The same methods and precautions as described under input mode should be used for determining interrupt source.

Bit-Programmable Mode: The bit-programmable mode is entered by loading the control register (OUT 6) with the appropriate word from Table XVIII. A **SECOND LOAD TO THE CONTROL REGISTER MUST FOLLOW** with data to program the direction of each bit. Every 0 in the byte will assign that bit position as an input, a 1 as an output. If both ports were set at once (OUT 6, data = hex DB), the second load will set the direction of both ports simultaneously.

Once a port is in the bit-programmable mode, its STB and RDY lines can also be programmed as input or output data lines. (Except when port A is bi-directional; BSTB and BRDY are assigned to it). Table XX gives the control register (OUT 6) bits for setting STB and RDY line use. Bit 1 selects which port is to be acted on. Bit 2 high allows bit 6 to set the RDY line direction, while bit

3 high allows bit 7 to set the STB line direction.

All STB and RDY lines can be read on the status register (INP 6), regardless of programmed direction. See Table XIX.

If STB or RDY are output bits, they can be written with an OUT 6. Bit 1 selects port A or B, bits 4 and 5 are the RDY and STB output data, and the remaining bits are 0's.

Note that ARDY and BRDY are outputs when reset is applied. If connected as inputs, that is to some other driving source, at least 1000 Ohms should be placed in series. This prevents damage by excessive current flow between the RDY output and the external source when reset is applied.

In the bit-programmable mode, the CDP1851 can generate interrupts on logical combinations of input or output bits. Table XXI gives the interrupt control word (OUT 6) bit assignments. Bit 3 selects port A or B, bit 4 indicates if a new interrupt mask is to follow, and bits 5 and 6 select the applicable logic function. When bit 4 is set, **A SECOND LOAD TO THE CONTROL REGISTER (OUT 6) MUST FOLLOW**. Every bit in the mask that is a 0 feeds the corresponding bit position in the port to the interrupt logic. A mask of hex FF is not allowed.

Once interrupt conditions are set up, interrupts have to be enabled by loading the appropriate control word from Table XVIII. The CPU interrupt signal and/or bits 0 and 1 from the status register can then monitor the logical conditions of the unmasked data bits.

Bidirectional Mode: Only port A can be bidirectional, and only if port B is first placed in the bit-programmable mode. Port A now uses all 4 handshake lines. Table XVIII gives the appropriate control word.

The ASTB and ARDY lines function for input handshaking the same as in the input mode. BSTB and BRDY function as output handshaking, the same as in the output mode, with the addition of BSTB being a 3-state control. With BSTB high, the port A output drivers

Table XIX: Status Register Bit Assignments (INP 6)

Bit-Programmable Mode Only				Bidirectional Mode Only		Any Mode	
Bit 7	6	5	4	3	2	1	0
BSTB Input Data	BRDY Input Data	ASTB Input Data	ARDY Input Data	A INT. Source = ASTB	A INT. Source = BSTB	A INT. Request	B INT. Request

Table XX: STB and RDY Line Control Bit Assignments (Out 6)

Bit 7	6	5	4	3	2	1	0
STB Direction	RDY Direction	STB Output Data	RDY Output Data	Set STB Function	Set RDY Function	Port Select	0
0 = STB = Input 1 = STB = Output 0 = RDY = Input 1 = RDY = Output				0 = Don't Change STB Function 1 = Set STB Direction as Bit 7		0 = Select Port A 1 = Select Port B 0 = Don't Change RDY Function 1 = Set RDY Direction as Bit 6	

are enabled.

Interrupts and CPU handshaking are the same as if both ports A and B were in use, except only the A interrupt request (status register bit 6) is active. To determine whether an input or output operation caused the interrupt, status register bits 2 and 3 must be checked. See Table XIX.

sets 4.9152 MHz, and pins 2 to 3 sets 2.4576 MHz. The selected clock is buffered and available on pin 13 of the backplane.

Not all available Microboards will accept the higher CPU speed. Table XXII gives presently available boards capable of running at the higher speed. Consult RCA for up to date information.

Table XXI: Interrupt Control Bit Assignments (Out 6)

Bit 7	6	5	4	3	2	1	0
0	Select Logic Function	Mask Follows	Port Select	1	0	1	
0 0 = Interrupt if Any Unmasked Bit is Low 0 1 = Interrupt if Any Unmasked Bit is High 1 0 = Interrupt if All Unmasked Bits are Low 1 1 = Interrupt if All Unmasked Bits are High			0 = Select Port A 1 = Select Port B	0 = No Change to Mask 1 = Next Byte is Mask*			

*Note: When Bit 4 is Set, a Second Out 6 Must Follow to Set Interrupt Mask: See Text

Setting Clock Speed

There are 2 selectable clock speeds. LK5, pins 1 to 2.

Table XXII: RCA Microboards with 5 MHz Capability

Memory	I/O
CDP18S628 32/64K RAM/ROM	CDP18S641B UART
CDP18S630 8K RAM	CDP18S651 Floppy Disk Controller
CDP18S631 16K RAM	CDP18S655 Real Time Clock
CDP18S632 32K RAM	CDP18S650 Counter/Timer

Selecting Alternate CPU's

Although supplied with a CDPI805A CPU, any presently available 1800 series CPU may be used. Link 15 pins 1 to 2 and Link 16 allows use of different CPU's, and allow enabling/disabling of internal memory on CDP1804's. See Table XXIII for setting Links 15 and 16. (LK15, pins 3 - 4 disables RNU.)

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Table XXIII: RCA CPU Selection

CPU	LK15	LK16
CDP1802, 1802A, 1802B	1 - 2	2 - 3, 4 - 5
CDP1805, 1805A, 1806, 1806A	—	2 - 3, 4 - 5
CDP1804A, no internal memory	—	2 - 3, 4 - 5
CDP1804A, with internal RAM/ROM	—	1 - 2, 5 - 6

Note that the RCA CDP1804A with internal memory enabled uses on-chip memory address decoders. The user must make sure that none of the CDP18S600 memory is linked for the same addresses.

Run Utility

The RNU (backplane pin 3) signal is "OR'ed" with address bit 15 for the on-board memory address decoding. RCA utility programs, such as CDP18SUT70, are located at address hex 8000, and can thus be entered from reset if RNU is held high.

RNU is pulled low through a resistor for systems not requiring this function. Noise immunity can be increased by tying RNU low with LK15, pins 3 - 4. Make sure LK15, pins 3 - 4, is open if an active RNU source such as the MS1M40 or CDP18S640A is present in the system.

Power-On Clear

An R - C integrator and a Schmitt trigger provide approximately a 180 MSec long CLEAR-N signal when the +5 volt supply is turned on. This open collector, active low signal appears on the backplane and the parallel interface connector, and is used to initialize the CPU, UART, and PIO. It also disables all memory chip selects, and the CPU, backplane and UART clocks. It does not reset the group select latch, nor stop the oscillator.

The CLEAR-N signal resets the UART interrupt flip-flop, receiver holding register, control and status registers, and sets SDO high (low at the RS232 interface). It also sets both PIO ports to input mode, resets the status register, drops both RDY lines, disables interrupts, and sets the interrupt mask register to all 0's (all bits enabled). It does not reset data already loaded in the PIO.

The CPU clear function has been discussed under "Microboard Bus Interface Signals".

If an external power-up reset or reset/RUN U source is available, such as on the MS1M40 supply and control module, the on-board power-up clear should be disabled. Link LK17 pins 1 - 2.

Using On-Chip RAM

The 64 byte RAM contained in the CDP1805A CPU (or the CDP1804A when internal decoding is disabled) may be accessed through an external decoder. LK15 pin 2 is the low-active memory enable input. LK 11, pins 6, 1, 3, and 4 are 4 decoded active low chip selects. An unused pin could be jumpered to the CPU memory enable input. See Tables IV, V, or VI for the 1 socket memory bank decoding. (The 64 byte RAM will "wrap around" to fill the entire 2, 4, or 8K decoded space.

Installation in Microboard Systems

The CDP18S600 may be installed in the CDP18S008, MS2000, or CDP18S693, 694, or 695 development system, or in the CDP18S670 or MSI series of industrial chassis. It is intended for use only in systems with a Microboard Universal Backplane. See each system manual for appropriate memory address requirements. The CDP18S600 may be run at its higher clock speed in the RCA MS2000 Micro Disk Development System with the standard board complement, thus increasing throughput. **Use in other systems or with non-designated boards requires use of the lower clock speed.**

Linking Summary

Table XXIV: Summary of System Link Connections

Link	Use	Referenced From
LK1	PIO and UART: flags and interrupts	Table XII
LK2, 3	CTS, SDI: select RS232, RS422	Table XIII
LK4	Set UART group number	Table X
LK5	Set CPU clock speed	Setting Clock Speeds
LK 6 - 10	Set U17 — 21 memory types	Tables II, IX
LK11, 14	Set U21 memory address	Tables III, IV, V, IX
LK12, 13	Set U17 — 20 memory addresses	Tables VI, VII, VIII, IX
LK15	Set CPU type, disable RUN Utility	Table XXIII, Run Utility
LK16	Set CPU type, use	Table XXIII
LK17	Disable power-on clear	Power-On Clear

Parts List

- | | |
|--|---|
| <p>C1, C2, C6, C9 - C15 = 0.1uf, ± 20%, 50V
 C3, C4 = 2.2 uf ± 20%, 20V
 C5 = 47 pf, ± 10%, 200V
 C7 = 10 pF, ± 10%, 200V
 C8 = 39 pF, ± 10%, 200V
 C16 = 4.7 uF, ± 10%, 10V
 CR1 = 1N914B Diode
 R1 = 10 Meg, ¼W, 5%
 R2 = 3K, ¼W, 5%
 R3, R5 = 10K, ¼W, 5%
 R4, R6 = 200 Ohm, ¼W, 5%
 R7 = 2.2K, ¼W, 5%
 R8 = 1.8 Meg, ¼W, 5%
 N1 = 10K, 8-pin resis. network
 N2, N4, N6 = 10K, 10-pin resis. network
 N3 = 10K, 6-pin resis. network
 N5 = 22K, 10-pin resis. network
 Y1 = 9.8304 MHz crystal
 S1 = pos. DIP switch
 J1, J2 = 10-pin rt. angle connector</p> <p>Mates with:
 Header: AMP No. 1-86148-2
 Contacts: AMP No. 1-87309-4
 Keying Plug: AMP No. 87077-1
 (supplied)</p> <p>U1 = CDP185ICE
 U2 = 9637ARM EIA Receiver
 U3 = 9638RM EIA Driver
 U4 = CA3240E
 U5, U6, U9 = CD40107BE
 U7, U10 = CD74HC14E</p> | <p>U8, U25, U31 = CD74HC75E
 U11 = CDP1854ACE
 U12 = CD74HC164E
 U13 = CD74HC74E
 U14, U26 = CD74HC02E
 U15 = 4702BPC Baud Rate Generator
 U16 = CD74HC245E
 U21 = HM6116IP-4 2Kx8 RAM
 U22 = CD74HC27E
 U23 = CD74HC11E
 U24, U27 = CPD1866CE
 U28 = CDP1805ACE
 U29 = CD74HC4075E
 U30 = CD74HC373E
 U32 = CD74HC367E
 Card Extractor - MS1A 11
 XU1, XU11, XU28 = Socket, 40-pin
 XU2, XU3, XU4 = Socket, 8-pin
 XU17 - XU21 = Socket, 28-pin</p> <p>P2 mates with a variety of 34-pin flat cable connectors such as T & B Ansley 609-3415M, Berg 65764-005, 3M 3463-0001, or equivalent (not supplied)</p> <p>Push-on links:
 AMP No. 531220-3
 Berg 76264-101
 or equivalent</p> |
|--|---|

RCA CMOS Microboard Computer CDP18S600

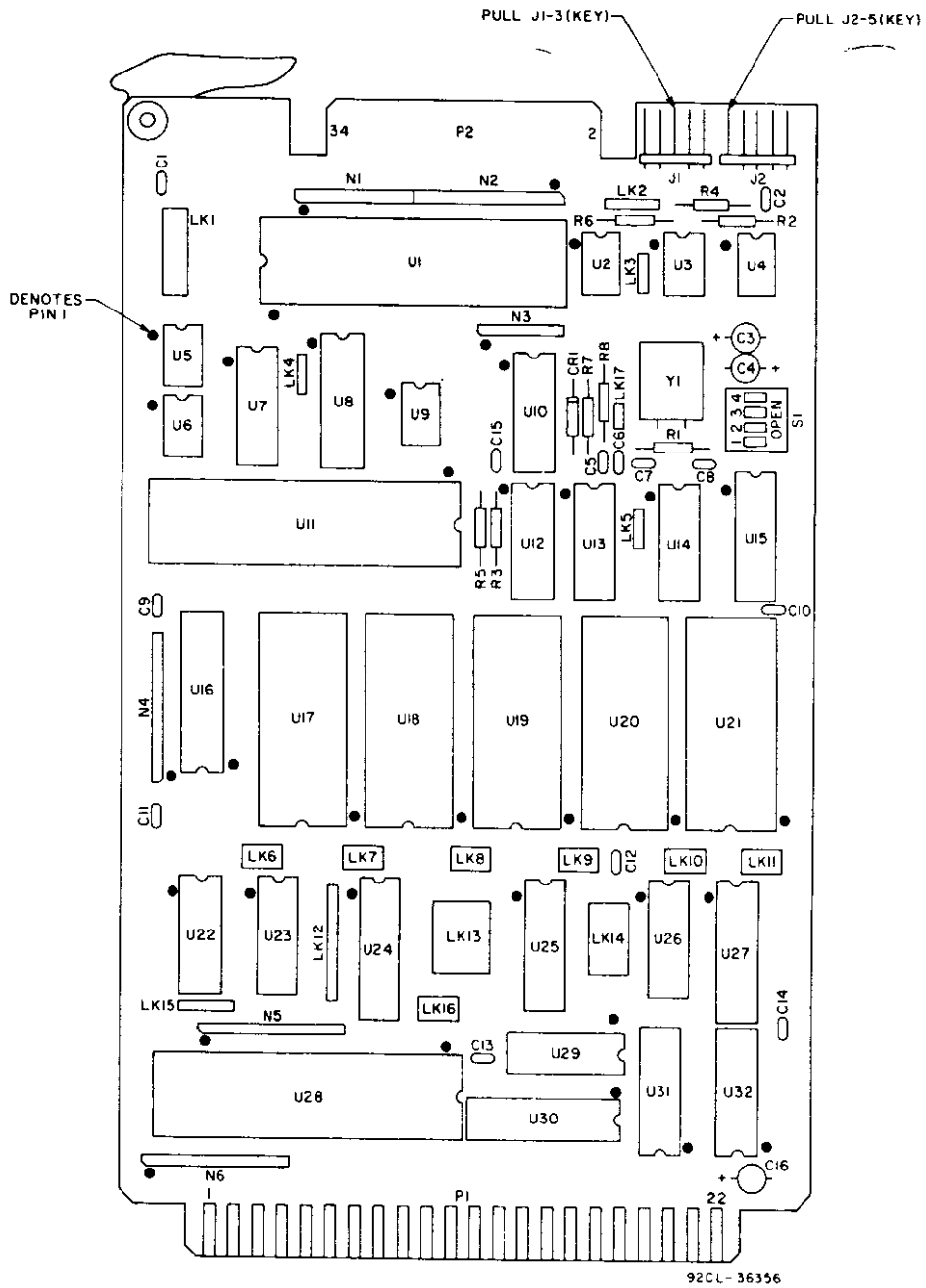


Fig. 6 - Microboard Computer CDP18S600
Layout Diagram.

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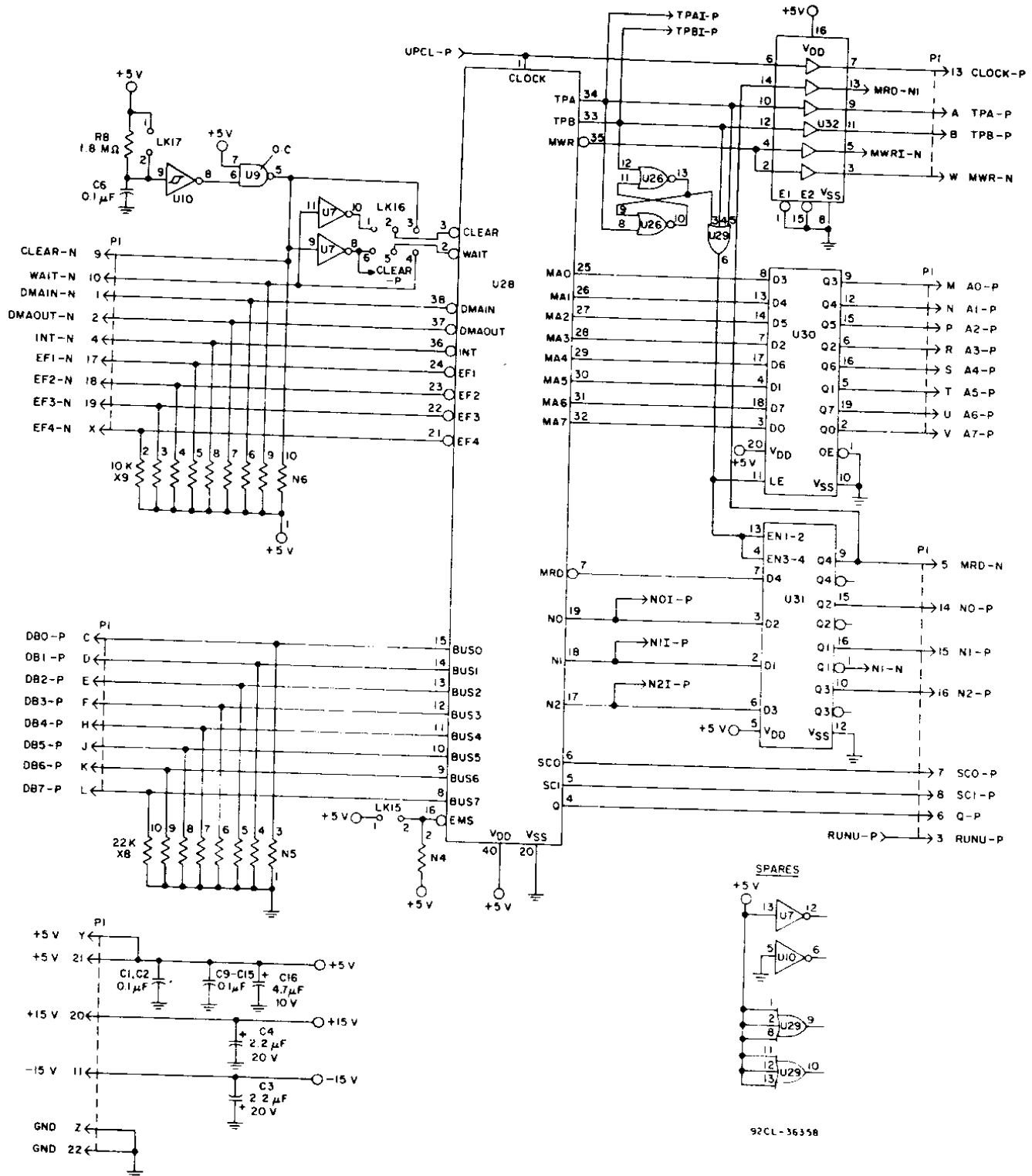


Fig. 7 - Microboard Computer CDP18S600 Logic and Circuit Diagram - Central Processor Unit.

RCA CMOS Microboard Computer

CDP18S600

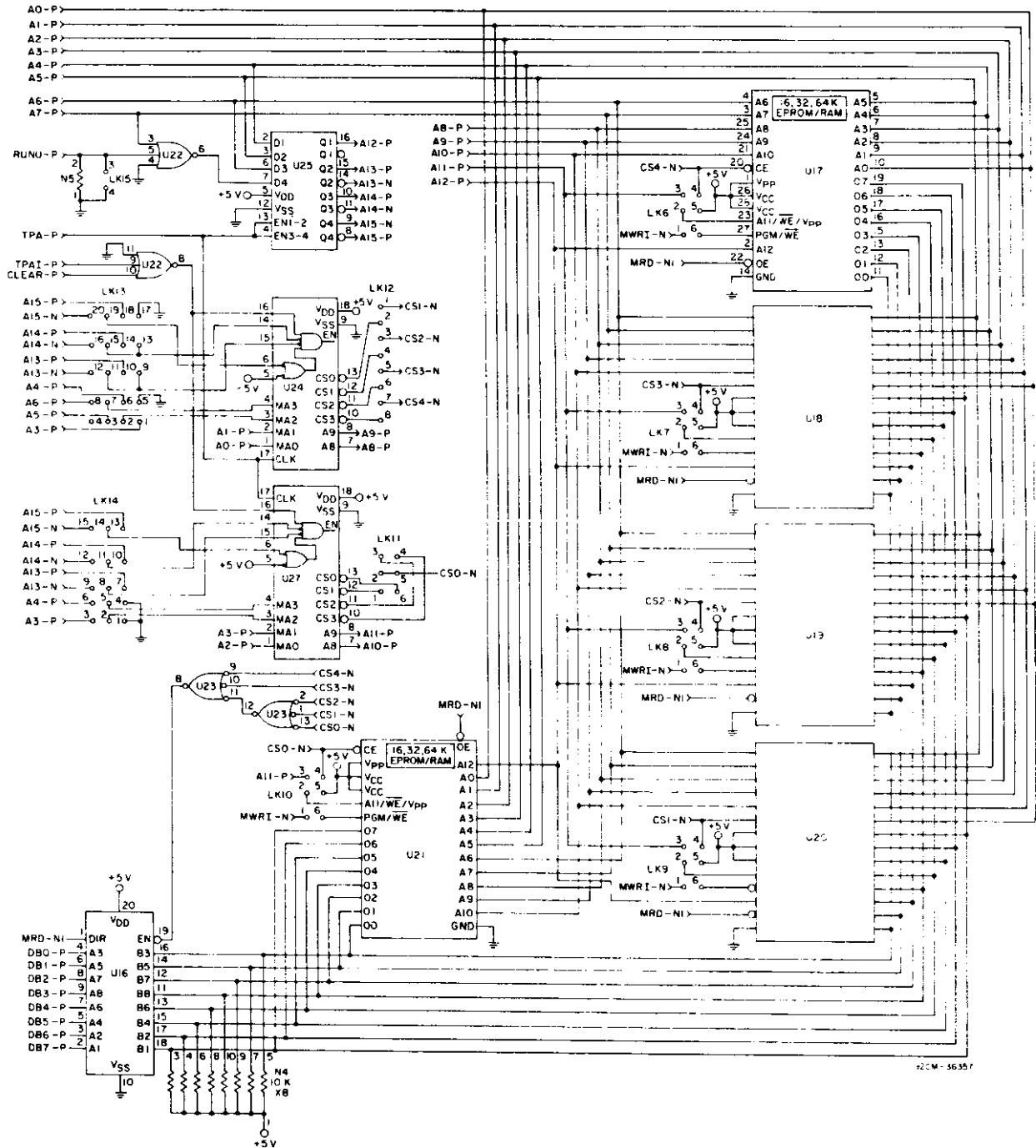


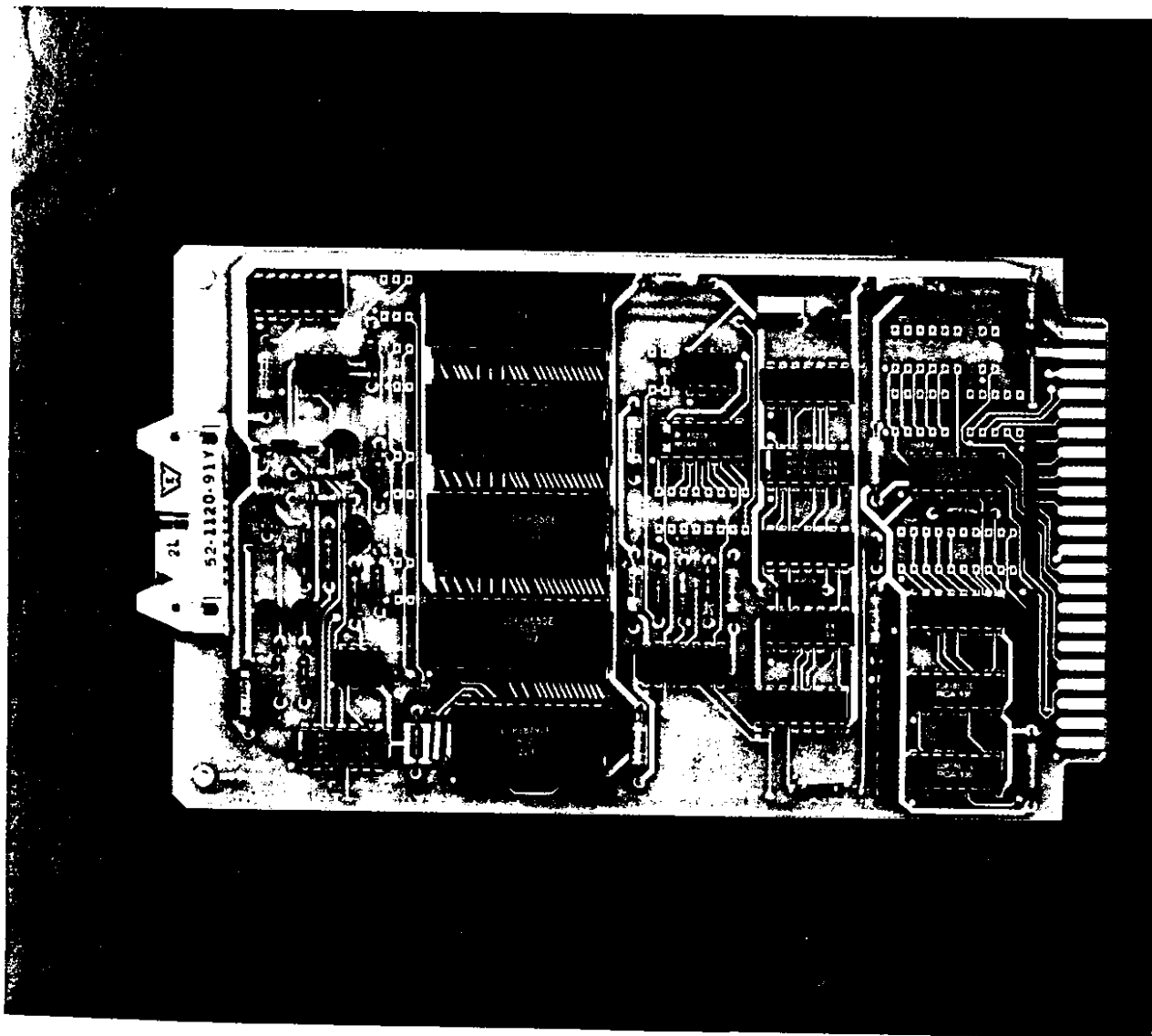
Fig. 8 - Microboard Computer CDP18S600 Logic and Circuit Diagram - Memory Portion.

SYSASSIST
ELECTRONIC SYSTEMS DIVISION

S-5579

Multiply/Divide/Clock Board

Microboard* Compatible



Trademark of RCA

S-5579

SYSASSIST

S-5579 MDU-Clock

Features

- Microsecond math processing
- 32 x 32 bit multiply operation
- 64/32 bit divide operation
- Time and date clock
- "Watchdog" timer reset
- Low power CMOS circuitry
- Alarm interrupt
- Timebase interrupt or flag
- Powerdown mode with automatic powerup
- External timer outputs
- External power connections
- 74HCxx devices permit highspeed bus operation

The Sysassist S-5579 Math Clock Board is a CMOS Microboard* compatible function board. The board is designed to be used with any of the extensive assortment of CMOS Microboards available from RCA. The S-5579 consists of both math and clock chips, providing a variety of features useful in a wide range of systems.

The S-5579 can be configured with 1 to 4 CDP1855 multiply/divide chips for math functions from 8x8 to 32x32 bits. Most configurations complete an operation in less than one microprocessor bus cycle. The math operations are fast enough for most real-time control

applications, including proportional control and velocity control loops in industrial machinery and robots.

The CDP1879 clock chip provides complete crystal-controlled clock functions suitable for time and date functions on larger systems, as well as providing real-time interrupts for smaller dedicated control systems. A special power-down feature is provided with complete power switching for up to one amp per supply (5, 15, -15) provided on the S-5579. An external power connector maintains clock power, permitting automatic power-up at a preset time. In remote data logging and telemetry applications, the math capability provides extremely rapid processing of data, which in conjunction with the power-down feature can provide low system duty cycles and low power consumptions. A "Wired-Or" input is provided which can override the power-down state if there are external conditions which require immediate attention. An automatic reset function is provided to periodically reset the processor in systems where program failure is unacceptable; the period is under software control. In systems where volatile memory must be maintained, a wait generator is provided which reduces power without turning off the system bus; a battery-backed RAM board is available from RCA if desired.

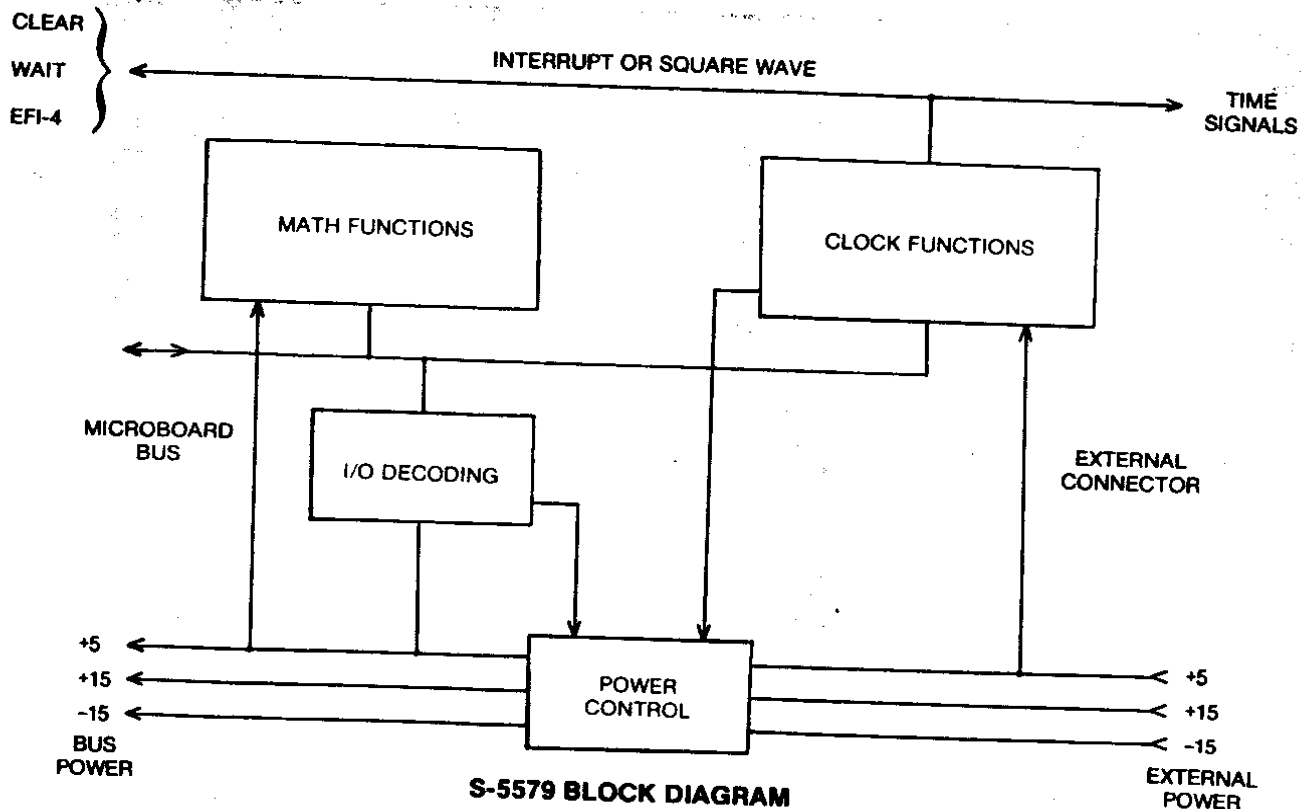


Fig. 1 — Math-Clock Block Diagram.

S-5579 Link Tables

NUMBER OF MUDs				
	1	2	3	4
LK2	1-4	OPEN	OPEN	OPEN
	2-3	OPEN	OPEN	OPEN
LK3	OPEN	1-4	OPEN	OPEN
	OPEN	2-3	OPEN	OPEN
LK4	OPEN	OPEN	1-4	OPEN
	OPEN	OPEN	2-3	OPEN

MATH CLOCK PRESCALER LINK 5		
1/4	1-6	SHORTED
1/2	2-5	SHORTED
1	3-4	SHORTED

OVERFLOW FLAG LINK 9		
O.F. to INT	1-10	SHORTED
O.F. to EF1	2-9	SHORTED
O.F. to EF2	3-8	SHORTED
O.F. to EF3	4-7	SHORTED
O.F. to EF4	5-6	SHORTED

WAIT RELEASE SOURCE LINK 7		
CLK	1-4	SHORTED
INT	2-3	SHORTED

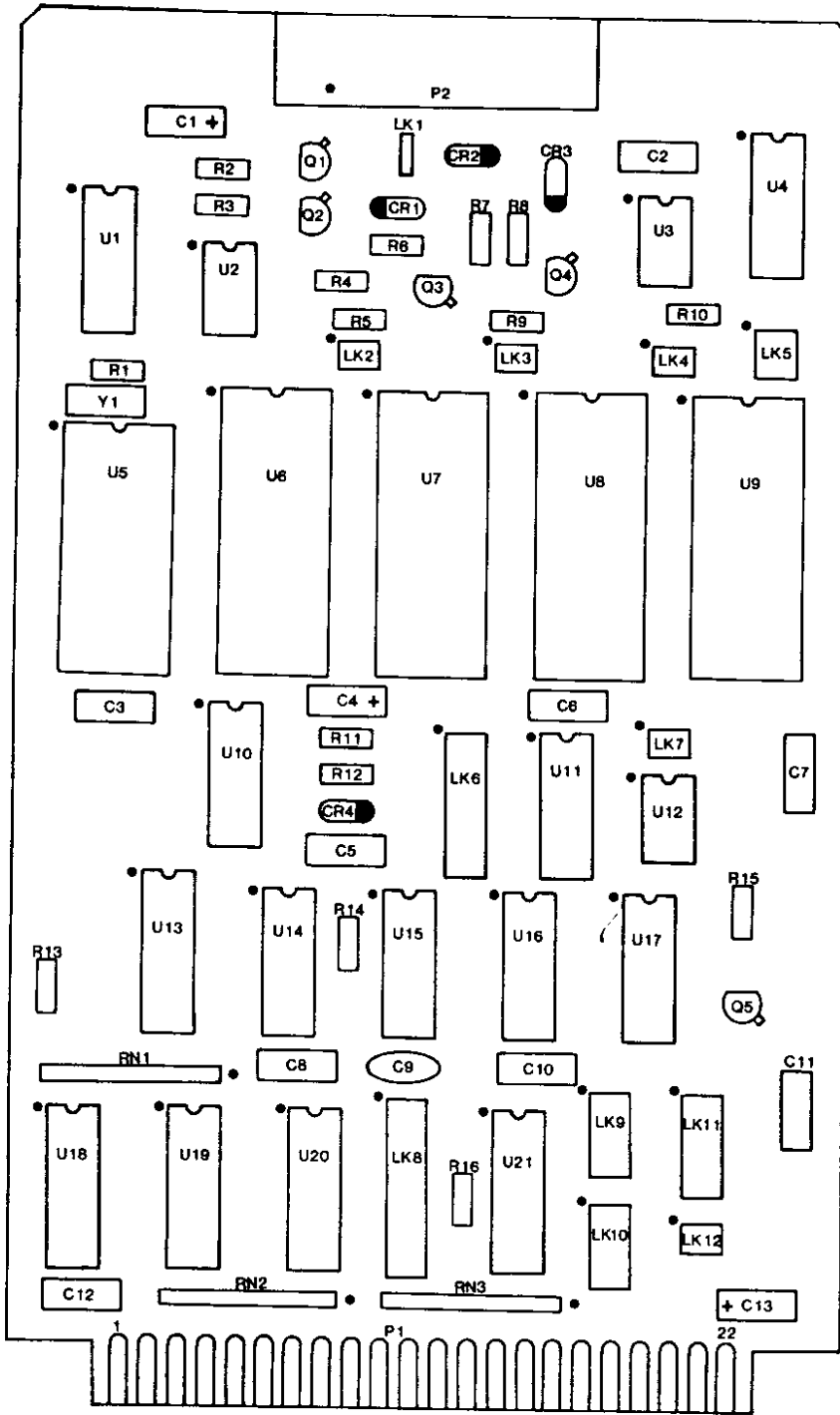
WAIT FUNCTION LINK 12		
CLEAR	1-4	SHORTED
WAIT	2-3	SHORTED

GROUP SELECTS LINK 8		
00-70H	6-10 4-12	SHORTED OPEN
80-FFH	4-12 6-10	SHORTED OPEN
1 of 8	PIN NUMBER	PREPRINTED LINKS
0	1	
1	2	POWERDOWN
2	3	MATH SELECT
3	4	CLOCK SELECT
4	5	WAIT GENERATE
5	7	
6	8	
7	6	

DEVICE SELECTS AT LINK 8	
PIN	DEVICE
19	POWERDOWN
18	MATH
17	CLOCK
16	WAIT GENERATOR

1879 CLOCK PULSE DESTINATION LINK 10		
INT	5-6	SHORTED
EF1	4-7	SHORTED
EF2	3-8	SHORTED
EF3	2-9	SHORTED
EF4	1-10	SHORTED

1879 INTERRUPT DESTINATION LINK 11		
INT	1-12	SHORTED
EF1	2-11	SHORTED
EF2	3-10	SHORTED
EF3	4-9	SHORTED
EF4	5-8	SHORTED
CLR	6-7	SHORTED



Parts List

- U1, 14, 16 = 74HC04
- U2, 3, 12 = 40107
- U4 = 74HC74
- U5 = 1879
- U6, 7, 8, 9 = CDP1855
- U10 = 74HC32
- U11 = 74HC164
- U13 = 74HC175
- U15 = 74HC00
- U17 = 74HC08
- U18, 19 = CDP1857
- U20 = 74HC138
- U21 = 4050
- CR1, 2, 3, 4 = 1N4001
- Q1, 2, 4 = 2N6732
- Q3, 5 = 2N6731
- RN1 = 20K
- RN2, 3 = 100K
- R1 = 1M, 1/4W
- R2 = 479 ohms, 1/4W
- R3 = 4.7K, 1/4W
- R4, 6, 13 = 1K, 1/4W
- R5, 9, 10, 11, 14, 15 = 20K, 1/4W
- R7, 8, 12 = 10K, 1/4W
- R16 = 100K, 1/4W
- C1 = 22uF @16v
- C2-8, C10-12 = 0.1 @50v
- C9 = .001uF
- C13 = 22uF @ 16v
- Y1 = 32.768 KHz
- P2 = RIGHT ANGLE HEADER

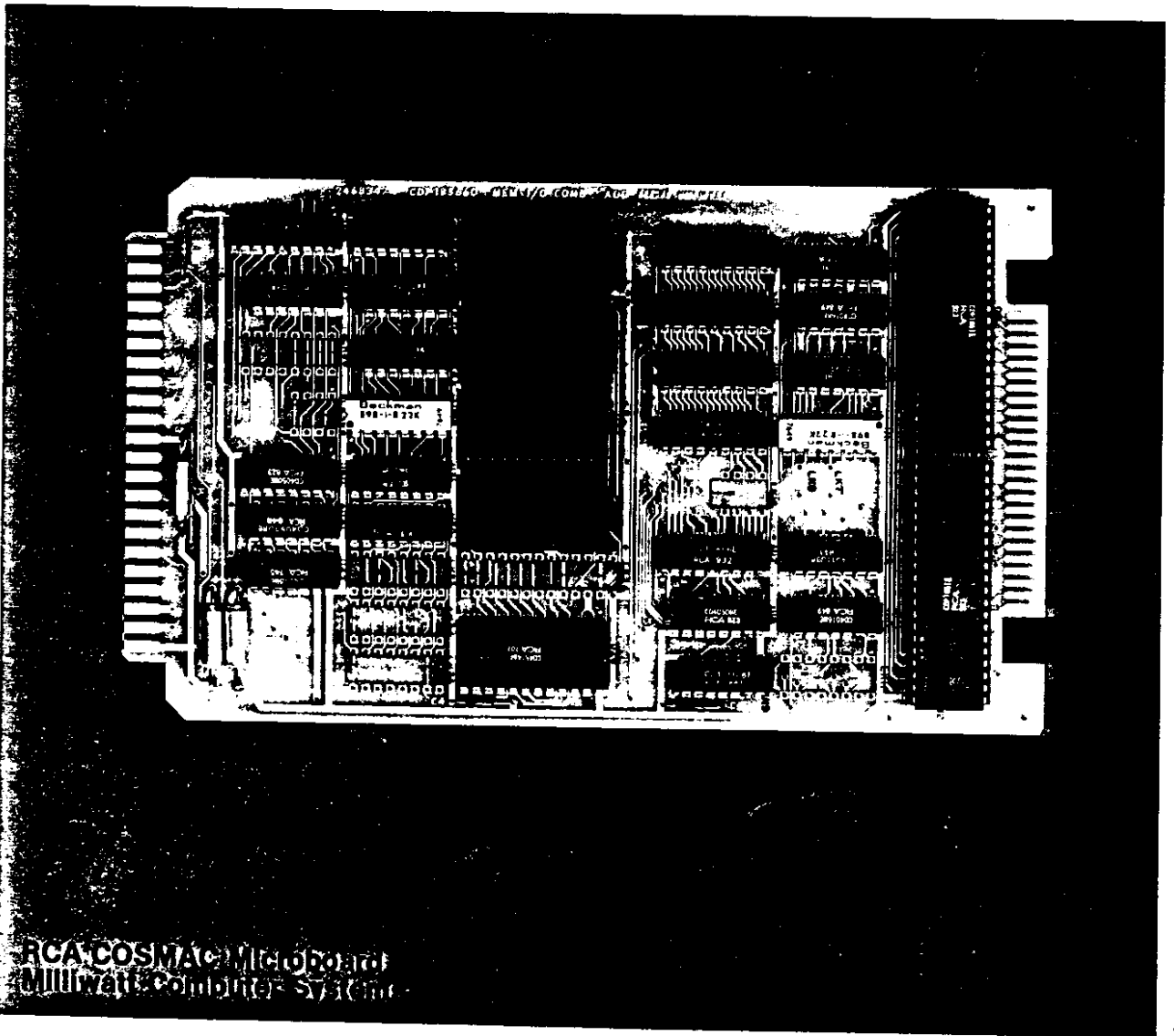
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RCA COSMAC Microboard Combination Memory and I/O Module

CDP18S660



RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660

The RCA COSMAC Microboard Memory and I/O Module CDP18S660 is a versatile expansion module combining RAM, ROM, and I/O lines. It contains two kilobytes of static CMOS RAM (4 MWS5114's), four on-board sockets for read-only memory (up to 8 kilobytes of EPROM for read-only memory (up to 8 kilobytes of EPROM for mask-programmable ROM), two CMOS programmable interfaces (CDP1851's), plus address latches and decoders and I/O latches and decoders. Address and data lines are buffered to minimize loading of the Microboard bus interface.

Specifications

Memory Capacity

On-board RAM: 2 kilobytes (4 CMOS static RAM's, 1024 x 4, MWS5114)

On-board ROM/EPROM: 4 sockets for up to 8 kilobytes (CDP1834, 2708, 2758, 2716)

Memory Address Map

On-board RAM: Any two 1-kilobyte blocks within any even 4-kilobyte block

On-board ROM/EPROM: Depending on type and quantity of ROM's, any 1-, 2-, 4-, or 8-kilobyte block

I/O Capacity

40 parallel lines programmable as input, output, or bidirectional

Operating Temperature Range

0°C to 70°C

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm)

Board pitch 0.5 inch (12.7 mm) minimum

Power Requirements

With CMOS ROM's: +5 V at 8 mA, typical operating

Features

- Low-power static CMOS
- Operable from single 5-volt supply
- High noise immunity
- Compatible with COSMAC Development Systems
- 2 kilobytes of read-write memory
- Sockets for 4/8 kilobytes of ROM/PROM
- 40 programmable I/O lines
- 44-pin system interface
- Expandable by use of COSMAC Microboard Universal Backplane
- Small board size: 4.5 x 7.5 inches
- RAM and ROM independently assignable within memory space
- Assignable I/O addresses
- Member of extensive Microboard family
- Simple system interface
- Temperature range: 0°C to 70°C

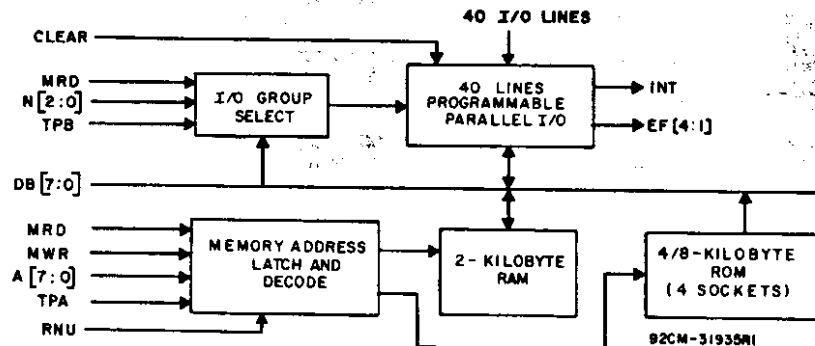
Connectors

System Interface: Edge fingers, 44 pins on 0.156-inch centers

I/O: Edge fingers, 50 pins on 0.100-inch centers

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660. For further information on



Block diagram of RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660.

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these signals, refer to the data sheet for the CDP1802 (File No. 1023) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201.**

DB7 through DB0

Eight bidirectional data bus lines. Taken directly from the Microboard Universal Backplane to the CDP1851 I/O devices, but buffered from the ROM and RAM memories by CDP1856's, these lines are used to transfer data between memory, CPU, and I/O devices.

A7 through A0

Eight memory address lines on which the high and low address bytes are multiplexed. The high-address byte is latched at the TPA trailing edge and used by the on-board decoders to select the appropriate block of memory.

TPA, TPB

Timing pulses generated by the CPU which occur once in each machine cycle. TPA trailing edge is used to latch the high-order memory address. TPB trailing edge is used to latch output data from the data bus.

\overline{MWR}

A WRITE command from the CPU to the memories. Address lines are stable at this time. Actual writing or latching occurs at the trailing edge.

\overline{MRD}

A READ command from the CPU to the memories and a direction indicator for I/O data transfers. In the I/O instructions it corresponds to N3 (N register, internal to the CPU) which distinguishes I/O inputs from outputs. \overline{MRD} must be used to condition output drivers in all memory components, or their output buffers, to avoid contention on the data bus. The absence of \overline{MWR} must not be interpreted as a READ. Early in a write cycle, data are being driven onto the data bus by the CPU or an input device. If a memory allows its outputs to be enabled while \overline{MRD} is false before \overline{MWR} appears, bus contention will occur resulting in unnecessary power dissipation and perhaps circuit failures. Operation using the Micromonitor CDP18S030 is impossible unless \overline{MRD} is properly used to condition data output.

$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$, $\overline{EF4}$

Four external flags taken to the CPU by way of the Microboard Universal Backplane. These flags can be tested in software by conditional branch instructions.

N0, N1, N2

Taken directly from the Microboard Universal Backplane, these lines indicate an I/O instruction is being executed. They are derived from the low-order

three bits of the N register during an I/O instruction execution only. They are low (false) at all other times. These bits form the primary address identifying the I/O device. Direction of transfer, derived from N3 internal to the CPU, is presented on the \overline{MRD} line. When high, \overline{MRD} indicates data transfer from the I/O to memory; when low, from memory to I/O.

INT

Connected to the Microboard Universal Backplane via optional links and driven by transmission gates, INT originates in the CDP1851 I/O devices. Interrupt causes a transfer of control from the current program counter to register 1. Interrupts may be inhibited by software. If Interrupt Enable (IE) is set, recognition of INT results in a completion of execution of the current instruction followed by an S3 machine state during which designators X and P are stored in CPU register T. Then, X is set to 2, P is set to 1, and IE is reset to 0. The S3 state lasts one machine cycle (eight clocks), after which processing resumes with R1 as the program counter.

RNU

Run Utility Software. This signal is supplied to force the most significant address bit true. As a result, the program start is at memory location 8000 instead of 0000.

CLEAR

This input signal is used on the RCA COSMAC Microboard Module CDP18S660 to reset the ports on both CDP1851's to the input mode and to reset the status register, A RDY, B RDY, and interrupt enable (disabling interrupts).

On-Board Memory Addressing

The high-order eight memory address bits are latched, decoded, and used for generating chip selects for on-board memories. A system of links is provided for placing RAM or ROM in the desired area of the 64-kilobyte address space. As an alternative, DIP switches can be readily installed in place of links that may require frequent changing.

RAM Address

The RAM on the CDP18S660 is two kilobytes of static CMOS RAM. The four high-order address bits (A15, A14, A13, A12) are latched and decoded, and a set of eight links is provided so that RAM can be positioned in any even 4-kilobyte block. The next two address bits (A11, A10) are further decoded, and a set of four links is provided to allow RAM to occupy any two

RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660

1-kilobyte blocks within the selected 4-kilobyte block. The board is shipped prelinked with RAM occupying 2 kilobytes of contiguous memory from 9000 to 97FF. To alter this configuration, the user should cut connections 6:11 and 3:14 in link LK33 and connections 4:5 and 3:6 in link LK16 and then install jumpers in accordance with Tables I and II.

ROM Address

Four 24-pin sockets are provided for user-programmed ROM's. Four ROM types are suitable: CDP1834 (1 kilobyte), 2708 (1 kilobyte), 2758 (1 kilobyte), and 2716 (2 kilobytes, Intel pin-out). the CDP1834 mask-programmable ROM can be used in combination with any of the other three types. No other combination may be used. One to four ROM devices may be used.

Two types of links are provided to select the desired ROM configuration. The first link type is for accommodating the type of ROM selected. The second link type is for selecting the memory address space to be occupied by ROM.

Links LK24 and LK39 are 10-pin and 8-pin dual-in-line arrangements, respectively, with preprinted links to accommodate the CDP1834 or 2708 ROM's. Table III gives the connections required for each ROM type.

Links LK34 and LK35 are 16-pin dual-in-line arrangements. Link LK34 provides the high-order four address bits decoded so that two links or jumpers place sockets XU22 and XU23 in any 4-kilobyte block within the 64-kilobyte memory address space. Link LK35 does the same for sockets XU20 and XU21. Links LK34 and LK35 are prelinked so that ROM occupies 4 kilobytes of contiguous memory from 1000 to 1FFF. To alter the ROM address configuration, the user should cut pin connections 1:16 and 6:11 in links LK34 and LK35 and install jumpers in accordance with Table I.

To avoid having floating inputs to the gates, both links LK34 and LK35 should always have two jumpers. For example, if sockets XU20 and XU21 are unused, LK35 may be jumpered the same as LK34. Otherwise, spurious chip selects may be generated, turning on the three-state data buffers and causing interference with normal processing.

For 1-kilobyte ROM's such as the CDP1834, 2708, or 2758, links LK34 and LK35 should be jumpered identically in accordance with Table I. Then, ROM's should be installed in sockets XU23, XU21, XU22, and XU20, in that order, starting with the lowest-address ROM.

For 2-kilobyte ROM's (2716), links LK34 and LK35 should be jumpered independently in accordance with Table I for the required two 4-kilobyte blocks. Then,

Table I — 4-Kilobyte Link Connections

4-Kilobyte Address Space	Link LK33, LK34 or LK35 Pin Connections
0000-0FFF	1:16, 5:12
†1000-1FFF	1:16, 6:11
2000-2FFF	1:16, 7:10
3000-3FFF	1:16, 8:9
4000-4FFF	2:15, 5:12
5000-5FFF	2:15, 6:11
6000-6FFF	2:15, 7:10
7000-7FFF	2:15, 8:9
8000-8FFF	3:14, 5:12
†9000-9FFF	3:14, 6:11
A000-AFFF	3:14, 7:10
B000-BFFF	3:14, 8:9
C000-CFFF	4:13, 5:12
D000-DFFF	4:13, 6:11
E000-EFFF	4:13, 7:10
F000-FFFF	4:13, 8:9

LK33 is associated with the 2-kilobyte RAM
LK34 is associated with ROM sockets XU23 and XU22
LK35 is associated with ROM sockets XU21 and XU20
†Prewired ROM location on LK34 and LK35
‡Prewired RAM location on LK33

Table II — RAM 1-Kilobyte Link Connections
(2 required)

1-Kilobyte Address Space	Link LK16 Pin Connections	RAM Locations
X000-X3FF	*4:5	U12, U14
X400-X7FF	*3:6	U13, U15
X800-XBFF	2:7	U12, U14
XC00-XFFF	1:8	U13, U15

X denotes any one 4-kilobyte block (X = 0 to F), as fixed by link LK33
*Prewired links

socket XU23 is the low 2 kilobytes and socket XU22 is the high 2 kilobytes of the 4-kilobyte block as set in LK34. Similarly, socket XU21 is the low 2 kilobytes and socket XU20 is the high 2 kilobytes of the 4-kilobyte block set in LK35.

One-kilobyte ROM type CDP1834 is the only one that may be used in combination with 2-kilobyte ROM type

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Table III — ROM Type Selection Links

Link LK24 Pins	CDP1834*	2708*	2758	2716
1:10	X	OPEN	SHORTED	SHORTED
2:9	X	SHORTED	OPEN	OPEN
3:8	X	OPEN	SHORTED	OPEN
4:7	X	OPEN	OPEN	SHORTED
5:6	X	SHORTED	OPEN	OPEN
Link LK39 Pins				
1:8	OPEN	OPEN	OPEN	SHORTED
2:7	SHORTED	SHORTED	SHORTED	OPEN
3:6	OPEN	OPEN	OPEN	SHORTED
4:5	SHORTED	SHORTED	SHORTED	OPEN

*X = don't care; Links LK24 and LK39 are prewired to accept CDP1834 or 2708.

2716. If all links are set up for the 2-kilobyte ROM's as shown in Table III for LK24 and LK39, and if LK34 and LK35 are set up for different 4-kilobyte blocks, then a 1-kilobyte ROM in socket XU23 will occupy the two lower 1-kilobyte segments of the 4-kilobyte block. In other words, its 1 kilobyte will "wrap" through the lower 2 kilobytes of the 4-kilobyte block. If it is in socket XU22, it will wrap through the upper 2 kilobytes of the 4-kilobyte block. A 2-kilobyte ROM may be placed in either socket XU23 or socket XU22 while the other is occupied by a 1-kilobyte ROM. Socket XU21 (low 2 kilobytes) and socket XU20 (high 2 kilobytes) may be used in the same manner.

Note: When 2708 ROM's are used, the Microboard Universal Backplane must supply +12 volts on pin P1-20 and -5 volts on pin P1-11.

I/O Operation

Two-Level I/O Addressing Conventions

During the I/O instruction, the CPU presents the low-order three bits of its N register on the N2, N1, and N0 lines. N3 generates the MRD signal to indicate the direction of data flow. Thus, the instructions 61 through 67 and 69 through 6F provide seven output and seven input commands. These instructions may be interpreted by the system as either different commands to the same I/O device or as I/O commands to different devices as addressed by the N lines.

In a larger system more addresses are needed. In the Microboard system the following conventions are established.

1. The 61 output instruction is used to transmit a group number. The output data byte is latched and decoded by any Microboard module in the system having an I/O function.
2. The group number is divided into two parts, the lower four bits being a one-of-four encoding and the higher four bits being binary encoded. Thus, the number of addresses provided is 15 binary-encoded plus 4 individual lines, times the six commands left after reserving the 61 and 69. The total of useful I/O addresses is 114.
3. The 69 instruction is reserved for reading the latched output of the 61 instruction. The CDP18S660, however, does not provide this feature.

The use of the two halves of the group number must be independent and exclusive. That is, the high-order bits must be zero when any of the low-order bits is used, and the low-order bits must be zero when the high-order bits are used. Once a group is set up, subsequent 62-through-67 and 6A-through-6F instructions are recognized only by the devices assigned to that group number.

The CDP18S660 encodes the high four bits of the transmitted group number to select both CDP1851 programmable I/O interfaces. Each CDP1851 is assigned its own unique group number by jumpering the pin connections in link LK25 as shown in Table IV. The board is shipped prelinked with group number 10 assigned to U1 and group number 20 assigned to U2.

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RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660

Table IV — I/O Group Selects

Group Number	LK25 Pin Connections	
	U1	U2
10	*1:16	1:15
20	2:16	*2:15
30	3:16	3:15
40	4:16	4:15
50	5:16	5:15
60	6:16	6:15
70	7:16	7:15
80	8:16	8:15
90	9:16	9:15
A0	10:16	10:15
B0	11:16	11:15
C0	12:16	12:15
D0	13:16	13:15
E0	14:16	14:15

*Prewired links

I/O Interface

The I/O interface consists of 40 lines provided on connector P2. Each CDP1851 programmable I/O interface generates 20 lines: 8 lines for port A, 8 lines for port B, and 4 handshaking lines. These lines may be programmed as input, output, or bidirectional individually or as a block. The P2 connector also provides a logic ground and +5 volts to be used as a reference.

For more detailed information on the Programmable I/O Interface CDP1851, refer to the data sheet for that device (File No. 1056).

As previously described, each CDP1851 is assigned to a unique group number by jumpering the proper pin connections in link LK25 (see Table IV). The CDP1851 designated U1 is prelinked for I/O group 10. The CDP1851 designated U2 is prelinked for I/O group 20. Therefore, in order to enable access, a 61 output instruction with data = 10₁₆ or 20₁₆ is required before read, write, or control I/O may be performed.

Signals 1A RDY, 1B RDY, 2A RDY, and 2B RDY conditioned by the group select can generate flags EF1 through EF4 by jumpering the appropriate pin connections in link LK11 (see Table V). The board is shipped prelinked so that the selection of U1 conditions 1A RDY and 1B RDY, causing the generation of EF1 and EF2, respectively. Similarly, the selection of U2 conditions 2A RDY and 2B RDY, also causing the generation of EF1 and EF2 respectively.

Interrupts can be generated by signals 1 INTA and 1 INTB by jumpering link LK8. Signals 2 INTA and 2INTB can also be used to generate interrupts by

jumpering link LK7. If both links are jumpered, any of the signals 1 INTA, 1 INTB, 2 INTA, or 2 INTB will generate an interrupt.

Once the group select is accomplished, N1 and N2 are used to address the selected CDP1851. The following read and write instructions are used to access data, status, and command registers.

- 62 - Write to control register
- 64 - Write to Port A data register (if A is an output)
- 66 - Write to Port B data register (if B is an output)
- 6A - Read status register
- 6C - Read Port A data register (if A is an input)
- 6E - Read Port B data register (if B is an input)

Using the Ready Lines for Data Synchronization

When the group select for U1 is set, Port 1A and Port 1B RDY lines are presented to the CPU EF1 and EF2 lines as prelinked. When the group select for U2 is set, Port 2A and Port 2B RDY lines are presented to the CPU EF1 and EF2 lines as prelinked. For altering the CPU flag selection, see Table V. Note that there is a logic reversal: when RDY is true, the EF is false. A test for RDY true might use the B1 instruction (34) which would take the branch if RDY were false. Even though these RDY lines are primarily intended for "handshaking" with the device on the other end of the cable, they are useful for synchronizing data transfer between the CDP1851 and the CPU.

When a port designated as an output port is loaded, RDY goes true. When the receiving device takes the data, it transmits STB which removes RDY. The software can then test RDY until it is false (EF1 or EF2 true) and load the next output byte. When a port is designated as an input port, reading the data sets RDY, and the transmitting device resets RDY when it transmits data and STB. Again, the software tests to see if RDY is false and reads the input byte. In this case, a dummy read after reset is necessary to raise the first RDY.

Table V — CPU Flag Generation (Link LK11)

CDP1851 Signal Causing Flag Generation	Link LK11 Pin Connection			
	EF1	EF2	EF3	EF4
1A RDY	*8:9	—	6:11	—
1B RDY	—	*7:10	—	5:12
2A RDY	*4:13	—	2:15	—
2B RDY	—	*3:14	—	1:16

*Prewired links

Note that if the remote device is passive, such as a display or a set of points, handshaking is not necessary. The output port may be loaded at any time to change data without acknowledgment from the remote device. Similarly, the input port may be read at any time to store the current state of the input lines.

transmit data in both directions, using the input handshaking lines to synchronize inputs and the output handshaking lines for the output data. Operation is much the same as for independent input and output ports except that data is gated into AD0-AD7 only when the OUTPUT STB line is raised. In summary, Port A in the bidirectional mode is an output port and an input port sharing the same eight data lines, each having a set of handshaking lines.

Using the Interrupt Line for Data Synchronization

If links LK7 and LK8 are jumpered, 1 INTA, 1 INTB, 2 INTA, or 2 INTB generates INT to the CPU. INT is not conditioned by the group select. INT is set by the remote sending device STB to acknowledge an output port and is reset by loading an output port. Similarly, INT is set by the remote device sending STB to load an input port and is reset by reading the input port. Table VI summarizes the actions of READY and INT for input and output modes.

Bit-Programmable Mode

In each CDP1851, both Port A and Port B are capable of being programmed to be in the bit-programmable mode. Port B must be in this mode if Port A is in the bidirectional mode. In the bit-programmable mode, each line in AD0-AD7 and B0-B7 is programmed to be either input or output. In addition, the handshaking lines are programmed to be input or output lines unless Port A is bidirectional, in which case it uses all four handshaking lines. The handshaking lines, when used as data lines, are accessed by a write control for output lines and read status for input lines. The other eight lines in each port are accessed by the usual read and write data instructions.

The software can find the source of the interrupt by setting the appropriate group select and then either testing the RDY lines or reading the status byte. Depending on the group select, the low-order two bits of the status byte are:

bit 0 = 1 INTA or 2 INTA; bit 1 = 1 INTB or 2 INTB.

Interrupts are generated when an input line goes true except that the former handshaking lines cannot generate interrupts. The bits may be individually masked so as not to generate interrupts. The interrupt control word selects one of the two interrupt rules, AND or OR. The AND rule results in an interrupt only when all unmasked lines are true. The OR rule results in an interrupt when any unmasked line is true. The interrupt control word also defines the input lines as logically true when high or logically true when low.

Bidirectional Mode

In each CDP1851, Port A may be programmed to be bidirectional. In this case, Port B must be programmed to be in the bit-programmable mode, to be described later. In the bidirectional mode, A RDY and A STB become A INPUT RDY and A INPUT STB; BRDY becomes A OUTPUT RDY, and B STB becomes A OUTPUT STB. Each of the eight lines AD0-AD7 may

Table VI — READY and INTERRUPT Actions for Input and Output Modes

		Output Port	Input Port
READY	Set by Reset by	Loading Data STB leading edge	Reading Data STB leading edge
INTERRUPT	Set by Reset by	STB trailing edge Loading Data	STB trailing edge Reading Data

RCA COSMAC Microboard Combination Memory and I/O Module CDP18S660

*Pin Terminals and Signals
for the RCA COSMAC Universal Backplane
Connector (P1)*

Pin	Signal	Pin	Signal
A	TPA-P *	1	DMAI-N
B	TPB-P *	2	DMAO-N
C	DB0-P *	3	RNU-P *
D	DB1-P *	4	INT-N *
E	DB2-P *	5	MRD-N *
F	DB3-P *	6	Q-P *
H	DB4-P *	7	SC0-P *
J	DB5-P *	8	SC1-P *
K	DB6-P *	9	CLEAR-N *
L	DB7-P *	10	WAIT-N *
M	A0-P *	11	-5V/ -15 V *
N	A1-P *	12	SPARE
P	A2-P *	13	CLOCK OUT
R	A3-P *	14	N0-P *
S	A4-P *	15	N1-P *
T	A5-P *	16	N2-P *
U	A6-P *	17	EF1-N *
V	A7-P *	18	EF2-N *
W	MWR-N *	19	EF3-N *
X	EF4-N *	20	+12 V/ +15 V *
Y	+5 V *	21	+5 V *
Z	GND *	22	GND *

*Signals used on RCA COSMAC Microboard
Combination Memory and I/O
Module CDP18S660

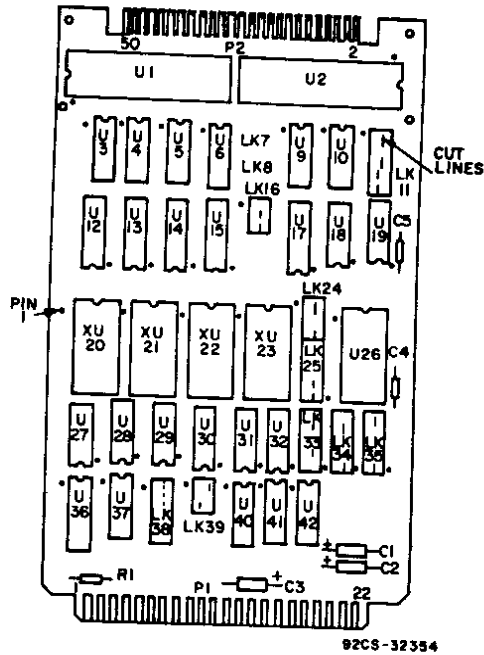
*Pin Terminals and Signals for the
Microboard I/O Connector (P2)*

Pin	Signal	Pin	Signal
1	2A STB-P	2	2A RDY-P
3	2AD1-P	4	2AD0-P
5	2AD2-P	6	GND
7	2AD3-P	8	GND
9	2AD4-P	10	2AD5-P
11	2AD7-P	12	2AD6-P
13	2B7-P	14	2B6-P
15	2B5-P	16	2B RDY-P
17	2B4-P	18	2B STB-P
19	2B3-P	20	2B0-P
21	2B2-P	22	2B1-P
23	GND	24	GND
25	GND	26	GND
27	GND	28	GND
29	1B1-P	30	1B2-P
31	1B0-P	32	1B3-P
33	1B STB-P	34	1B4-P
35	1B RDY-P	36	1B5-P
37	1B6-P	38	GND
39	+5 V	40	1B7-P
41	1AD6-P	42	1AD7-P
43	1AD5-P	44	1AD4-P
45	1AD0-P	46	1AD3-P
47	1A STB-P	48	1AD2-P
49	1A RDY-P	50	1AD1-P

NOTE: The signals on connector P2 come from
the two CDP1851 Programmable I/O Interfaces.
For electrical characteristics refer to the data
sheet for the CDP1851 (File No. 1056).

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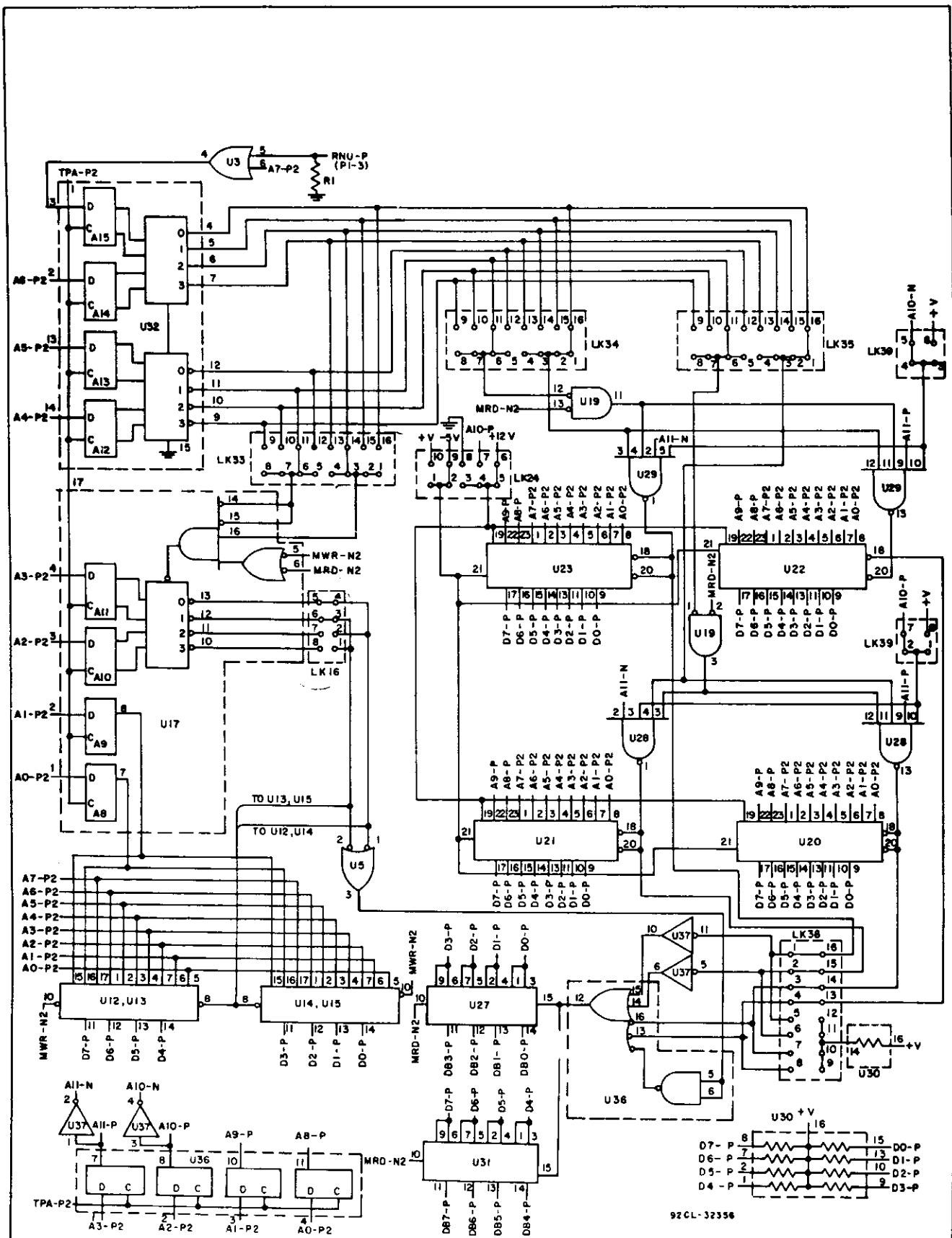


Parts List

- C1, C2, C3 = 15 μ F, 20 V
- C4, C5 = 0.1 μ F, 50 V
- R1 = 22 k Ω , 1/4 W
- U1, U2 = CDP1851CE
- U3 = CD4071BE
- U4, U10 = CD4016BE
- U5 = CD4011BE
- U6, U30 = resistor module 22 k Ω
- U9, U19 = CD4001BE
- U12-U15 = MWS5114E
- U17 = CDP1866CE
- U18, U40 = CD4050BE
- U26 = CD4514BE *5.5T LATCH / 4-0 16 Jumper*
- U27, U31 = CDP1856CE
- U28, U29 = CD4012BE
- U32 = CDP1858CE
- U36 = CDP1867CE
- U37, U41 = CD4069BE
- U42 = CD4073BE
- XU1, XU2 = 40-pin socket
- XU20-XU23 = 24-pin socket

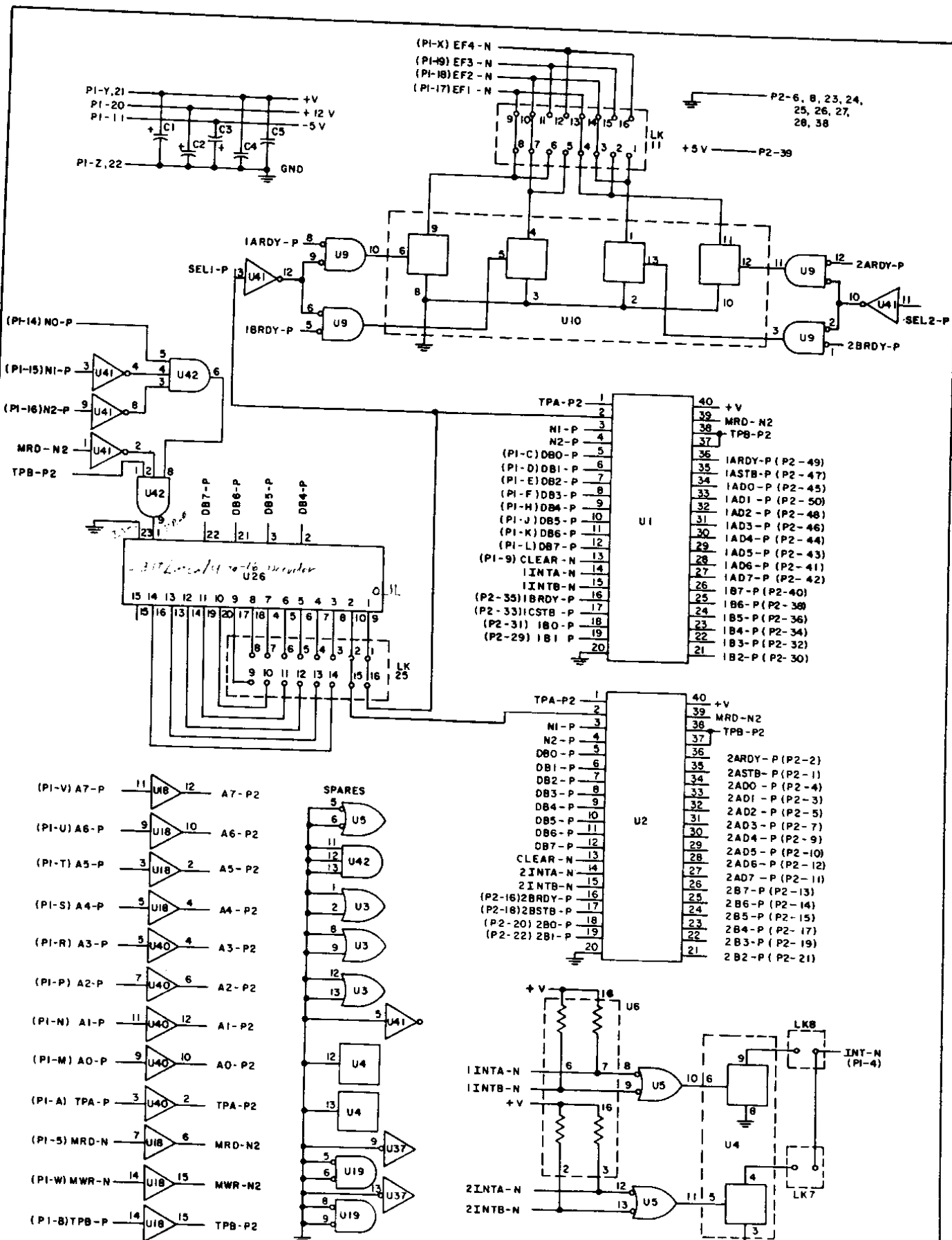
Layout diagram of RCA COSMAC Microboard
Combination Memory and I/O Module CDP18S660

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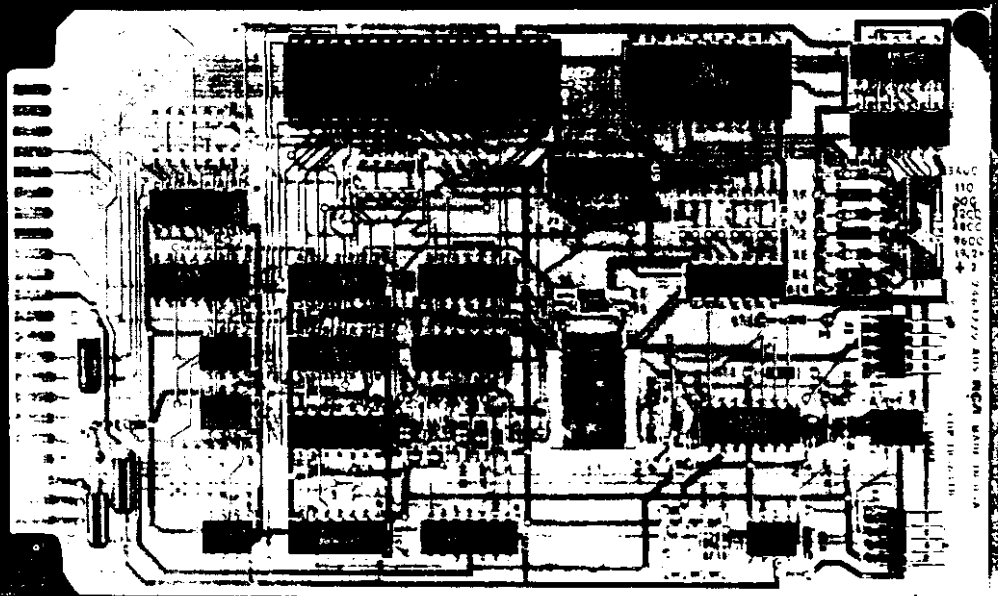
Logic diagram of Microboard Combination Memory and I/O Module CDP18S660 — memory portions.



Logic diagram of Microboard Combination Memory and I/O Module CDP18S660 — I/O portions.

92CL-32355

RCA Microboard UART Interface CDP18S641B



RCA Microboard
Milliwatt Computer Systems

RCA Microboard UART Interface

CDP18S641B

The RCA Microboard UART (Universal Asynchronous Receiver Transmitter) Interface Module CDP18S-641B is a parallel-to-serial I/O data controller utilizing the RCA CDP1854A UART. The CDP18S641B is designed for use in a Microboard computer system. The CDP18S641B provides an efficient byte interface to the system while serial data are transmitted and received at the remote interface. Baud rates from 110 to 19,200 are switch-selectable. It provides for full-duplex operation.

The CDP18S641B also provides two-level I/O address latching and decoding on board, with selectable addresses for flexible system configurations.

The CDP18S641B is plug-in compatible with the RCA MSI Series of Industrial Chassis and with RCA Microboard Computer Development Systems (MCDS) CDP-18S693 and CDP18S694 and Color CMCDS CDP18S-695 to facilitate hardware and software development. It can also be used with RCA Prototyping Systems CDP-18S691 and CDP18S692, and RCA Development Systems CDP18S005 (CDSII) and CDP18S007 (CDSIII).

Specifications

UART

CDP1854A, programmed mode.

Parity

Even or odd, or inhibited.

Stop Bits

One or two.

Word Length

5, 6, 7, or 8 bits.

Baud Rate

Crystal-controlled, switch-selectable for 55, 110, 150, 300, 600, 1200, 2400, 4800, 9600, or 19,200 baud.

Addressing

I/O space, link-selectable for both N codes and I/O group number.

Serial Interface

20-mA loop or RS232C.

Operating-Temperature Range

-40°C to +85°C

Power Requirements

Voltage (V)	With EIA	With 20-mA
	RS232C Terminal	Loop Terminal
+5	2 mA	2 mA
-5 to -15	7.5 mA	38 mA
+12 to +15	8.5 mA	40 mA

Features

- Low-power static CMOS
- High noise immunity
- Small board size (4.5 x 7.5 inches)
- Member of extensive Microboard family
- Compatible with RCA MSI Series of Industrial Chassis and RCA 1800-Series Development Systems
- Flexible address assignment
- Selectable baud rate
- Selectable serial interface: RS232C or 20-mA loop
- Paper-tape-reader run control
- Temperature range: -40°C to +85°C

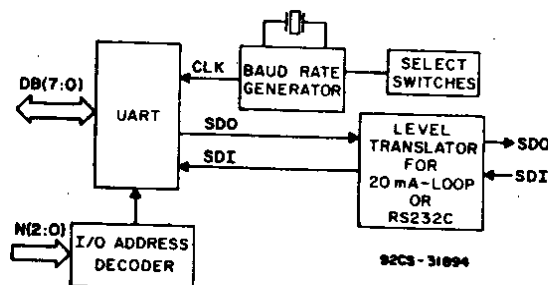
Connectors

System interface: Edge fingers, 44 pins on 0.156-inch centers.

Serial interface: Two right-angle 10-pin headers housing — AMP 1-86148-2
contact — AMP 86016-1
keying plug — AMP 87077-1

Dimensions

4.5 inches x 7.5 inches (114.3 x 190.5 mm);
Board pitch - 0.5 inch (12.7 mm) minimum.



Block diagram of RCA Microboard
UART Interface CDP18S641B.

Microboard Bus Interface Signals (Connector P1)

The following signals are generated or received by the RCA Microboard UART Interface Module CDP18S641B and provide the interface to other Microboard Systems components. For further information on these signals, refer to the data sheet for the CDP1802 (File No. 1305) and to the **User Manual for the CDP1802 COSMAC Microprocessor, MPM-201**.

Table I provides a list of the pins and the signals for the RCA Universal Backplane Connector signals marked with an asterisk (*) are those used on the RCA Microboard UART CDP18S641B.

DB7 through DB0 — These eight bidirectional data bus lines communicate directly with the CDP1854A UART, which has internal controls to establish direction and timing. In addition, DB7 to set the paper-tape-reader control, and DB7 through DB0 are used, through a system of optional links, to define the I/O group chosen for this board.

N0, N1, N2 — The N lines, which define the primary I/O address, are wired to a CDP1853 decoder. The CDP-

1853 outputs 7 through 1 are connected through optional links to the CDP1854A UART.

MRD — The Memory Read line is used by the CDP-1854A UART to identify proper direction of data flow on the bidirectional data bus. When true, this line indicates that data are being read from memory and, therefore, written to the I/O device, if an I/O operation is in progress. The direction is reversed when MRD is false.

TPA — This timing pulse is used only by the N decoder to set its output enable at the trailing edge of TPA.

TPB — This timing pulse is used by the CDP1854A UART to latch data written to it. It is also used by the N decoder to terminate its output enable at the trailing edge of TPB.

INT — This signal may be connected by optional link LK24 pins 1 and 14 to the INT output from the CDP1854A UART. This signal is buffered by a transmission gate so that wired-"OR" connection may be made with other devices driving the backplane INT line.

EF1, EF2, EF3, EF4 — Links are provided (link LK24) so that these flag lines may be wired to outputs from the CDP1854A UART. The outputs are Data Available (DA), Transmitter Holding Register Empty (THRE),

Table I — Pin Terminals and Signals for the RCA Universal Backplane Connector (P1)

Wire Side				Component Side			
Pin	Mnemonic	Signal Flow†	Description	Pin	Mnemonic	Signal Flow†	Description
A	TPA-P*	Out	System Timing Pulse 1	1	DMAI-N	In	DMA Input Request
B	TPB-P*	Out	System Timing Pulse 2	2	DMAO-N	In	DMA Output
C	DB0-P*	In/Out	Data Bus	3	RNU-P	—	Run Utility Request
D	DB1-P*	In/Out	Data Bus	4	INT-N*	In	Interrupt Request
E	DB2-P*	In/Out	Data Bus	5	MRD-N*	Out	Memory Read
F	DB3-P*	In/Out	Data Bus	6	Q-P	Out	Programmed Output Latch
H	DB4-P*	In/Out	Data Bus	7	SC0-P	Out	State Code
J	DB5-P*	In/Out	Data Bus	8	SC1-P	Out	State Code
K	DB6-P*	In/Out	Data Bus	9	CLEAR-N*	In	Clear-Mode Request
L	DB7-P*	In/Out	Data Bus	10	WAIT-N	In	Wait-Mode Request
M	A0-P	Out	Multiplexed Address Bus	11	-5V/-15V*	—	Auxiliary Power
N	A1-P	Out	Multiplexed Address Bus	12	SPARE	—	Not Assigned
P	A2-P	Out	Multiplexed Address Bus	13	CLOCK OUT	Out	Clock from CPU Osc.
R	A3-P	Out	Multiplexed Address Bus	14	N0-P*	Out	I/O Primary Address
S	A4-P	Out	Multiplexed Address Bus	15	N1-P*	Out	I/O Primary Address
T	A5-P	Out	Multiplexed Address Bus	16	N2-P*	Out	I/O Primary Address
U	A6-P	Out	Multiplexed Address Bus	17	EF1-N*	In	External Flag
V	A7-P	Out	Multiplexed Address Bus	18	EF2-N*	In	External Flag
W	MWR-N	Out	Memory Write Pulse	19	EF3-N*	In	External Flag
X	EF4-N*	In	External Flag	20	+12V/+15V*	—	Auxiliary Power
Y	+5 V*	—	+5 V dc	21	+5 V*	—	+5 V dc
Z	GND*	—	Digital Ground	22	GND*	—	Digital Ground

*Signals used on RCA Microboard UART Interface CDP18S641B.

†Signal flow is with respect to the CPU board.

92CS-34444R1

reading status from the UART, if the user does not wish to connect the links for status or interrupt. Connections for selecting interrupt or any of the status bits may be identified on the logic diagram.

Microboard computer system except that the Development System backplane must have certain signals wired to the UART location. The user should select an empty slot in the I/O section (slots 19 and 20 should be avoided), and then install the following wires in that slot.

Installation in the RCA Development Systems CDP18S005 (CDS II) and CDP18S007 (CDS III)

Installation in the CDS II (CDP18S005) or the CDS III (CDP18S007) is the same as for installation in a

- Pin 9 to pin 13 RESET-OP
- Pin 14 to Slot 13 pin 14 N0-P
- Pin 15 to Slot 13 pin 15 N1-P
- Pin 16 to Slot 13 pin 16 N2-P

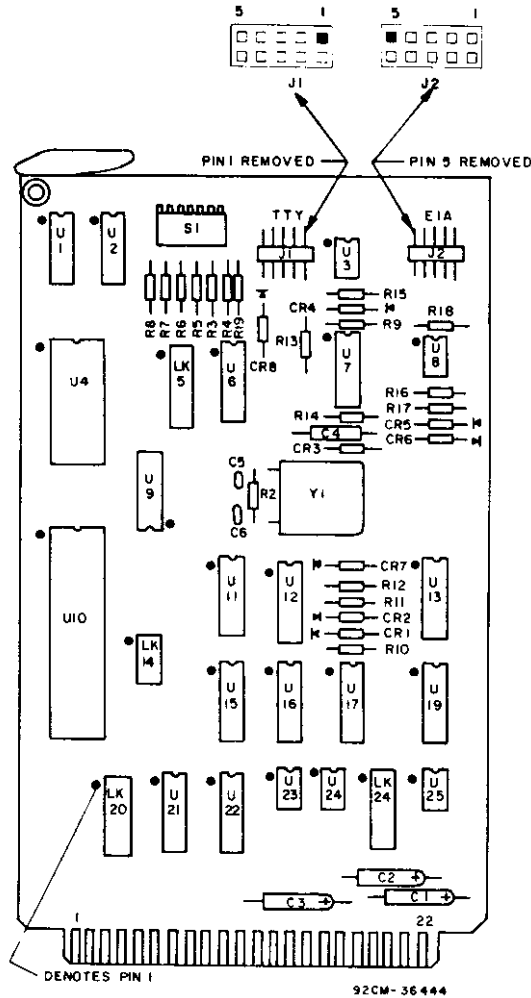
Table II — I/O Group Select Link Connections

I/O Group	LK5								LK14				
	1-16	3-14	5-12	7-10	2-15	4-13	6-11	8-9	1-10	2-9	3-8	4-7	5-6
01	O	O	O	S	S	S	S	O	O	O	O	O	S
02*	O	O	O	S	S	S	S	O	O	O	O	O	S
04	O	O	O	S	S	S	S	O	O	O	O	O	S
08	O	O	O	S	S	S	S	O	O	O	O	O	S
10	O	O	O	S	S	S	S	O	O	O	O	O	S
20	O	O	O	S	S	S	S	O	O	O	O	O	S
30	O	O	O	S	S	S	S	O	O	O	O	O	S
40	O	O	O	S	S	S	S	O	O	O	O	O	S
50	O	O	O	S	S	S	S	O	O	O	O	O	S
60	O	O	O	S	S	S	S	O	O	O	O	O	S
70	O	O	O	S	S	S	S	O	O	O	O	O	S
80	O	O	O	S	S	S	S	O	O	O	O	O	S
90	O	O	O	S	S	S	S	O	O	O	O	O	S
A0	O	O	O	S	S	S	S	O	O	O	O	O	S
B0	O	O	O	S	S	S	S	O	O	O	O	O	S
C0	O	O	O	S	S	S	S	O	O	O	O	O	S
D0	O	O	O	S	S	S	S	O	O	O	O	O	S
E0	O	O	O	S	S	S	S	O	O	O	O	O	S
F0	O	O	O	S	S	S	S	O	O	O	O	O	S

*Group 02 is preprinted. O = Open S = Shorted

RCA Microboard UART Interface

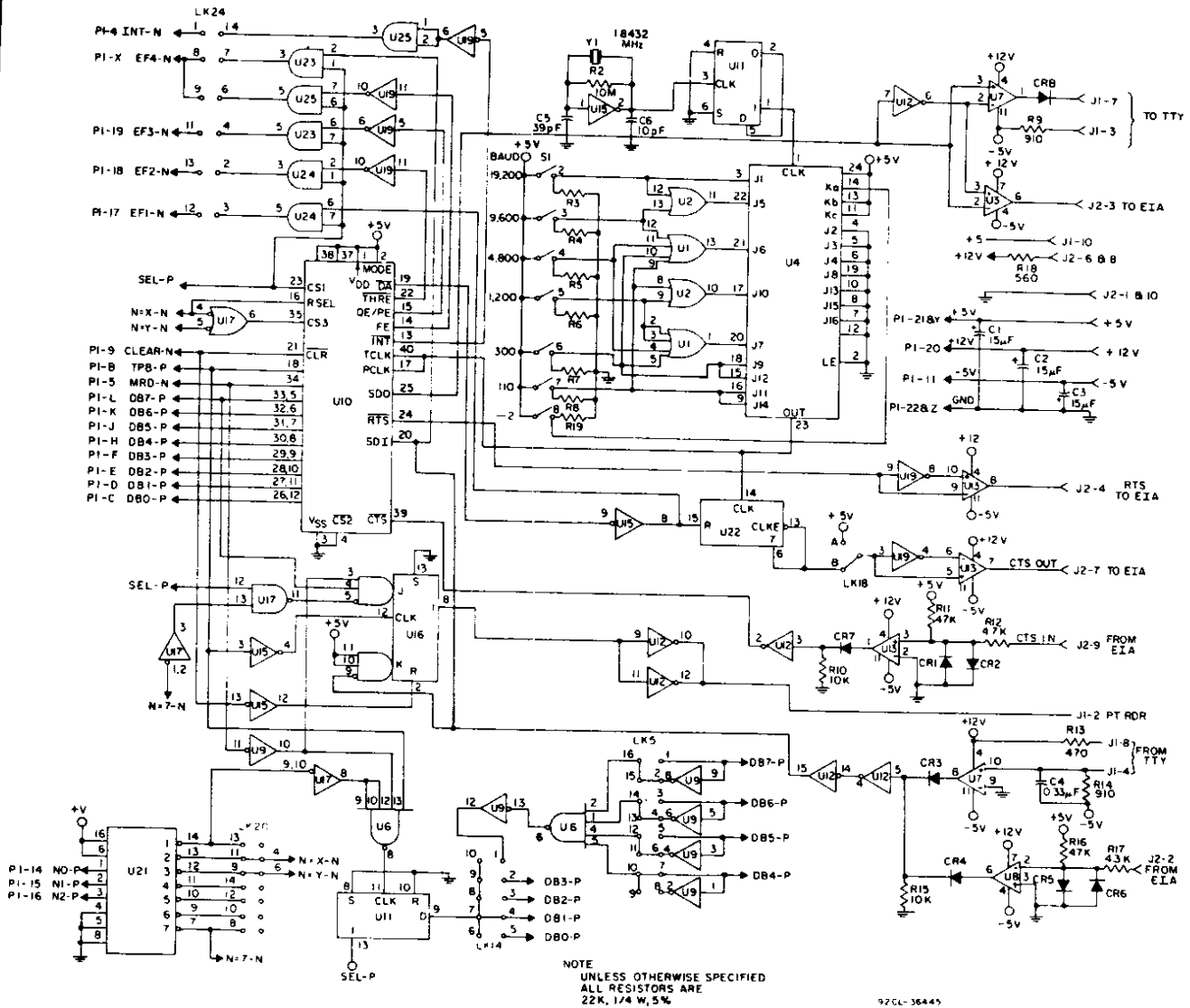
CDP18S641B



Layout diagram of RCA Microboard
UART Interface Module CDP18S641B.

RCA 1800

MICROSYSTEMS



Logic diagram of RCA Microboard UART Interface Module CDP18S641B.

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RCA Microboard UART Interface

CDP18S641B

Parts List

C1, C2, C3 = 15 μ F, 50 V

C4 = 0.33 μ F, 50 V

C5 = 39 pF,

C6 = 10 pF,

CR1 — CR8 = 1N914

J1, J2 = connector, right angle (mates with connector comprised of housing — AMP 1-86148-2, contact — AMP 86016-1, keying plug — AMP 87077-1, or equivalent)

R2 = 10 M Ω , ¼ W

R3-R8, R19 = 22 k Ω , ¼ W

R9, R14 = 910 Ω , ¼ W

R10, R15 = 10 k Ω , ¼ W

R11, R16 = 47 k Ω , ¼ W

R12 = 4.7 k Ω , ¼ W

R13 = 470 Ω , ¼ W

R17 = 4.3 k Ω , ¼ W

R18 = 560 Ω , ¼ W

S1 = 7-position DIP

U1 = CD4072BE

U2 = CD4071BE

U3, U8 = CA3140E

U4 = CD4059AE

U6 = 74HC20

U7, U13 = CA324E

U9 = 74HC04

U15, U19 = CD4069BE

U10 = CDP1854ACE

U11 = CD4013BE

U12 = CD4049BE

U16 = CD4096BE

U17 = 74HC00

U21 = 74HC138

U22 = CD4017AE

U23, U24, U25 = CD40107

Y1 = 1.8432-MHz crystal



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RCA Microboard UART Interface

CDP18S641B

Overrun Error or Parity Error (OE/PE), Framing Error (FE), and Serial Data In (SDI).

CLEAR — This signal provides an initialization signal for the CDP1854A UART and resets the paper-tape-motor control.

Operation

The operation of the RCA Microboard UART Interface CDP18S641B can be understood by reference to the logic diagrams. Reference should also be made to the technical data sheet (File No. 1193) for the CDP1854A UART (U10 on the logic diagram) for Mode 1 operation details.

The crystal-controlled oscillator circuit and the divide-by-N counter CD4059AE (U4) provide a clock for the UART at a frequency 16 times the rate selected by the user via the baud rate switch (S1), as required by the UART.

Switch position 1 and one of the switch positions 2 through 7 must be closed (down) to select the baud rate as marked. Switch position 1 may be opened (up) to divide the indicated baud rate by 2.

The clear-to-send-in signal CTS-IN from the connector J2 to the UART may be left floating, if desired, and it will assume the true state at the UART. The clear-to-send-out signal CTS-OUT is driven by the data available signal DA from the UART with a trailing edge delay. This signal may be used for handshaking, for example, between two UART modules. This output may be made true all the time by changing link LK18 to the A position.

Any communication with the UART Interface CDP18S641B or with any Microboard I/O Controller, must be started by the transmittal of the I/O group select number assigned to the controller. The system software transmits the group number by issuing an OUT1 (61₁₀) command whose data is the group number desired. This group number then stays selected until another OUT1 command supersedes it. Group number assignment details are given in the next section on **Installation**.

To operate the paper-tape reader, the system software should issue an output instruction 67 with the data byte containing a 1 in bit seven (most significant bit). The CD4096BE J-K flip-flop (U16) is triggered to the set state by this command, making the signal PT RDR low, thus enabling the tape reader. As soon as the reader starts to transmit data, the signal Serial Data In (SDI) causes the J-K flip-flop (U16) to be triggered to the reset state. As a result, one byte is transmitted to the UART and the tape is stopped before the next byte. Another 67 instruction, therefore, must be issued for each successive byte.

Installation in a Microboard Computer System

Installation of the Microboard UART Interface CDP18S641B in a Microboard Computer System requires only the setting of the proper baud rate switch (S1), as marked, unless the preselected addresses are not appropriate. The preselected addresses are as follows:

I/O GROUP	+ 02 ₁₀
DATA INPUT	+ INP2 (6A ₁₀)
DATA OUTPUT	+ OUT2 (62 ₁₀)
STATUS INPUT	+ INP3 (6B ₁₀)
CONTROL OUTPUT	+ OUT3 (63 ₁₀)
FLAG AND INTERRUPT LINES ARE OPEN	

A system of link positions is provided so that the user can select variations of the above functions. The links are arranged and numbered in a DIP configuration for ease of identification and to allow installation of DIP switches, headers, or other aids in the event frequent changes are anticipated.

For changes in the I/O group assignment, refer to Table II for links LK5 and LK14.

The primary addresses for data transfer and status/control transfer are prewired for Input/Output 2 and Input/Output 3, respectively. Should different I/O instructions be required, Link LK20 should be wired as follows.

For data transfer, wire link LK20 pin 4 to:

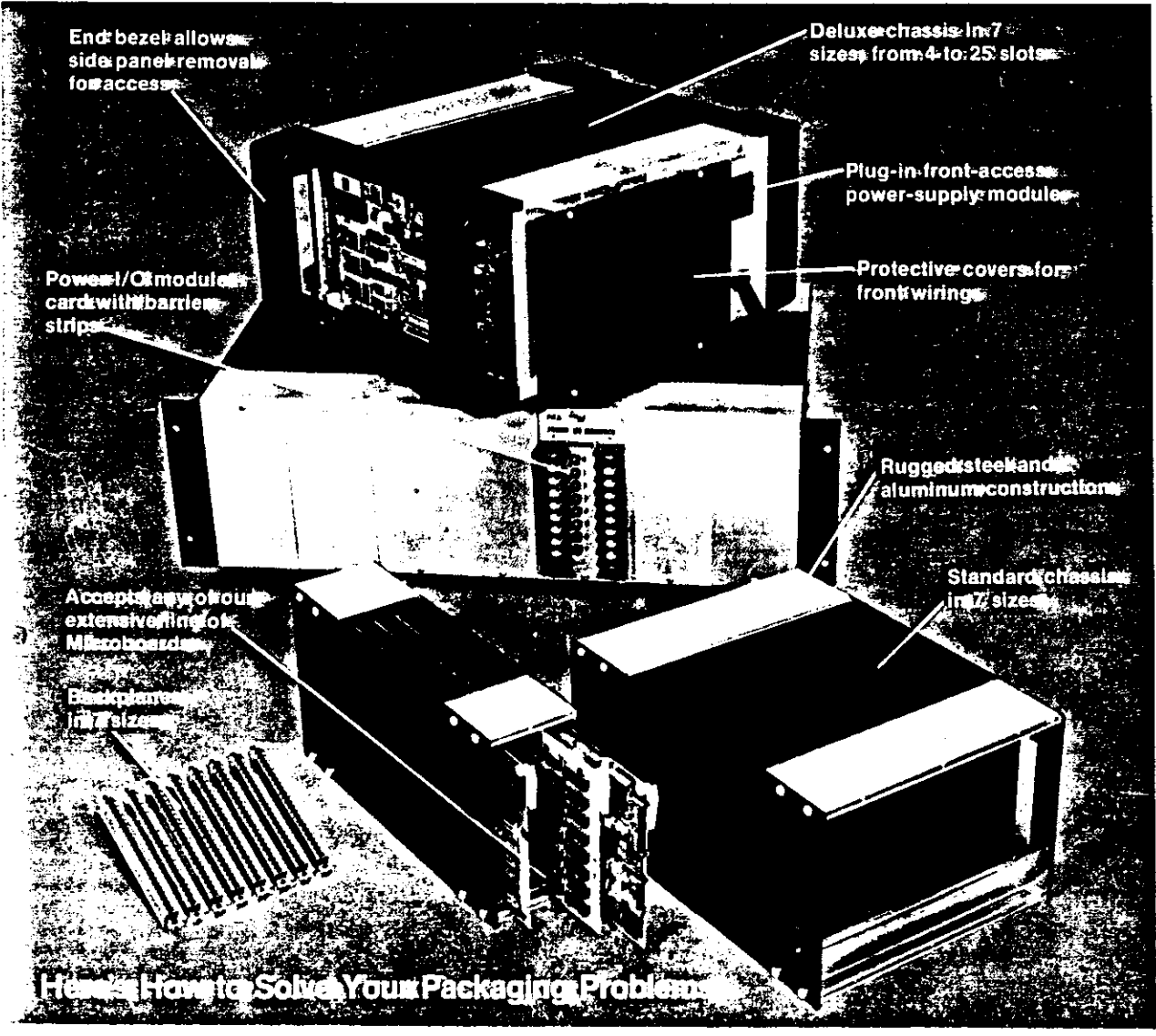
Pin 11 + INP 2, OUT 2
Pin 9 + INP 3, OUT 3
Pin 14 + INP 4, OUT 4
Pin 12 + INP 5, OUT 5
Pin 10 + INP 6, OUT 6
Pin 8 + INP 7, OUT 7

For status in or control out, wire link LK20 pin 6 to:

Pin 11 = INP 2, OUT 2
Pin 9 = INP 3, OUT 3
Pin 14 = INP 4, OUT 4
Pin 12 = INP 5, OUT 5
Pin 10 = INP 6, OUT 6
Pin 8 = INP 7, OUT 7

Link LK24 provides a means of connecting the UART interrupt to the system interrupt, as well as the UART status bits to the external flags EF1 through EF4 of the system. The interrupt is then unconditioned, but the flags are enabled by the group select. Thus, an interrupt-identification polling scheme may be implemented by system software. Polling may also be accomplished by

RCA Microboard Industrial Chassis Series



RCA Microboard Industrial Chassis Series

RCA's Microboard Industrial chassis series includes 21 chassis easily convertible, through a broad line of versatile accessories, to hundreds of different customer-selectable configurations for mounting on a rack, backwall, or desk, or in custom equipment.

They range from a simple backplane with connectors for four boards to a fully enclosed chassis with room for a plug-in power supply and 24 boards. Other sizes hold 8, 12, 16, 20, or 24 boards. Each unit can be customized with accessories to give you exactly what you want in a chassis.

- Rugged** — designed to stand up to tough industrial environments
- Flexible** — for system prototyping design and redesign
- Attractive** — desk-top configuration enhances any office
- Versatile** — mountable on 19" EIA rack, on backwall, or on surface
- Accessible** — provides front or side access to controls
- Efficient** — sizes available to accommodate up to 24 cards
- Easy to Use** — Microboard Universal Backplane
- Compact** — small CMOS Microboards, no bulky fans

**Table I —
Product Designations of RCA COSMAC Microboard Industrial Chassis Series and Associated Accessories.**

Chassis	
MSI 800 series	— Standard chassis
MSI 8800 series	— Deluxe chassis
MSI 8000 series	— Backplanes with connectors
Accessories	
MSIA 0100 series	— Solid top and bottom covers
MSIA 0200 series	— Perforated top and bottom covers
MSIA 0300 series	— Solid rear panels
MSIA 0400 series	— Front panel guards
MSIA 06	— Mounting angle brackets
MSIA 07	— End bezels (handles)
MSIA 08	— Four-card front panel
MSIA 10	— Cable conduit
MSIA 11	— Card extractor

Flexibility with Style — Deluxe Chassis MSI 8825

Includes all accessories shown

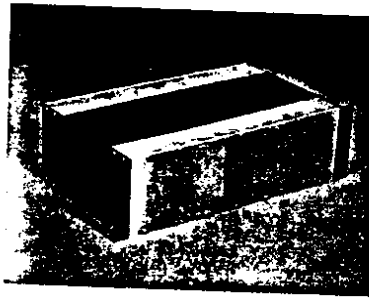


Photo A — Deluxe chassis MSI 8825 with angle brackets positioned for flush mounting in a 19-inch rack.

Photo B — Deluxe chassis MSI 8825 with front panel guard and angle brackets positioned for recessed mounting in 19-inch rack.

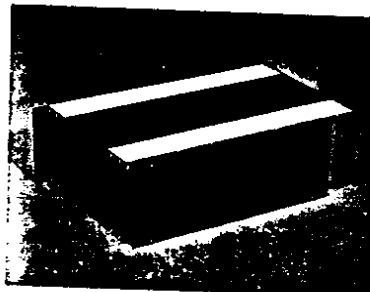
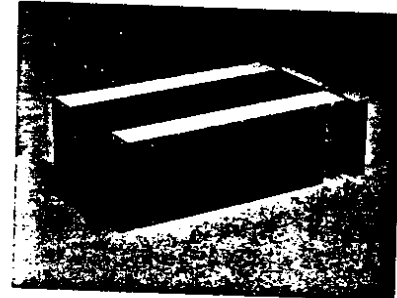


Photo C — Deluxe chassis MSI 8825 with front panel guard and angle brackets positioned for backwall mounting.

Photo D — Deluxe chassis MSI 8825 with end bezels (handles) and front panel guard for desk top use.

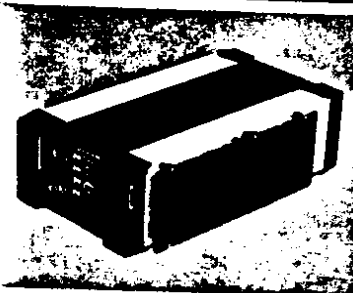
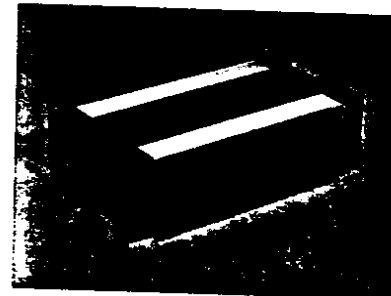


Photo E — Deluxe chassis MSI 8825 with end bezels (handles) and front panel guard. End panel removed to show CDP18S640 display and control Microboard module (available separately) in end position for access to controls.

The RCA COSMAC Microboard Industrial Chassis Series provides the designer with extremely flexible means of mounting, connecting, and enclosing the broad line of standard RCA Microboards as well as the newly developed RCA MSI-series Industrial Microboard products. The three series of industrial chassis available provide the user with both a wide range of option levels and a wide choice in the number of Microboard slots. One chassis series comprises a bare 44-pin Microboard backplane (MSI 8000); the second comprises a functional but unadorned chassis (MSI 800); the third comprises a complete chassis system that is fully enclosed, looks at home on a desk top, but is also rack or backwall mountable (MSI 8800). The Deluxe MSI 8800 series is the optimum starting point for packaging design.

Accessories are available to build the MSI 800 series at any option level up to that of the MSI 8800 series. See Tables I and II for model designations of the various chassis and accessories.

The basic unit of all series is 2.4 inches wide and accepts four Microboards (4.5 x 7.5 inches) on 0.6 inch pitch. Each series is available in 1 to 7 unit widths, with space for up to 24 Microboards. The 7-unit-wide model has a 25th connector dedicated to a plug-in power supply. The supply can mount in any other chassis, but occupies four slots.

The Standard MSI 825 (with optional MSIA 06 angle brackets) or the Deluxe MSI 8825 (angle brackets included) can be mounted in a 19-inch EIA rack, taking only 5-1/4-inch panel height. Flush or recessed mounting is possible. The brackets may also be used for backwall mounting of any of the MSI 800 or 8800 series chassis. See photos A, B, C, and K.*

The Deluxe MSI 8800 series is supplied with end bezels/carrying handles for portable or desk top use. The cover plate(s) under the end bezels may be omitted for access to the end card. This access allows the use of boards such as the CDP18S640 Control and Display Module or CDP18S480 PROM Programmer Module while the rest of the system is kept enclosed. See photos E and N. The end bezels are available as accessories for the Standard MSI 800 series.

*Photos G through P are on the back cover.

Features

- Rugged steel/aluminum frame — protective coating
- Microboard Universal Backplane
- Gold plated card edge connectors
- 0.062 inch FR4 epoxy backplane
- 4, 8, 12, 16, 20, 24, or 25 card slots
- Full-length card guides
- Extractor rails
- Access slots for ribbon cable
- Ample room within chassis for internal cabling
- Fully enclosed (MSI 8800)
- Rack or backwall mounting: only 5-1/4-inches high x 10.08 inches deep
- Flush or recessed rack mounting
- Protective see-through cover for wiring (MSI 8800)
- Desk-top use with carrying handles/end bezels (MSI 8800)
- Optional accessibility of end card (MSI 8800)
- Optional plug-in power supply (MSIM 40 or MSIM 40E)
- Optional power I/O interface module MSIM 20
- Connector for external supply
- Many accessories available: customize the chassis as needed
- Optional rack-mount wire trough front-panel wiring

*Apply to MSI 800 or 8800 Series.

Table II —
Designation Numbers for the Various Chassis

No. of Slots:	Standard Chassis	Deluxe Chassis	Backplanes With Connectors
4	MSI 804	MSI 8804	MSI 8004
8	MSI 808	MSI 8808	MSI 8008
12	MSI 812	MSI 8812	MSI 8012
16	MSI 816	MSI 8816	MSI 8016
20	MSI 820	MSI 8820	MSI 8020
24	MSI 824	MSI 8824	MSI 8024
25	MSI 825	MSI 8825	MSI 8025

MSI 800 Series: Standard Chassis

The MSI 800 series standard chassis have card guides and chassis added to the MSI 8000 series backplanes. See photo L and M. Front and rear aluminum extrusions have an alodine finish and are mounted to painted steel side pieces to give considerable structural strength. Spacer strips slide into the extrusions to locate full-length snap-in card guides. The connector tabs of the MSI 8000 backplane series slide into the rear extrusions, and nut plates slide into the front extrusions. Both are held captive by the side pieces. The nut plates provide for the mounting of MSI series industrial Microboards or matching MSIA 08 blank front panels. See Fig. 1 for dimensions.

A power supply connector is supplied loose with each chassis. For information see page 7. The chassis is electrically isolated from the Microboard backplane but may readily be grounded by connecting pin 22 or Z to a convenient chassis screw.

The side pieces have an entry slot for cable access to the front of the Microboards, but are reversible front to rear. If it is desired to mount and access the power-supply connector from the outside of the chassis, the left side piece should be reversed so that the entry slot is towards the rear.

Stick-on rubber feet are provided for desk-top use and are supplied loose.

A number strip along the inside of the bottom front extrusion identifies slot positions.

If the Microboards to be inserted in the chassis contain mounted standoffs, see the discussion under accessories for standoff removal. The standoffs will not clear the full-length card guides.

The MSI 800 series chassis will take any of the options listed in Table IV to bring it up partially or fully to the MSI 8800 deluxe chassis. Figs. 2 and 3 show mounting of optional accessories. Photo F shows a MSI 812 with available accessories. Refer to Fig. 4 for dimensions with optional end bezels or angle brackets. The MSI 825, which has slots for 24 Microboards, dedicates four additional right-most slots to power supply use.

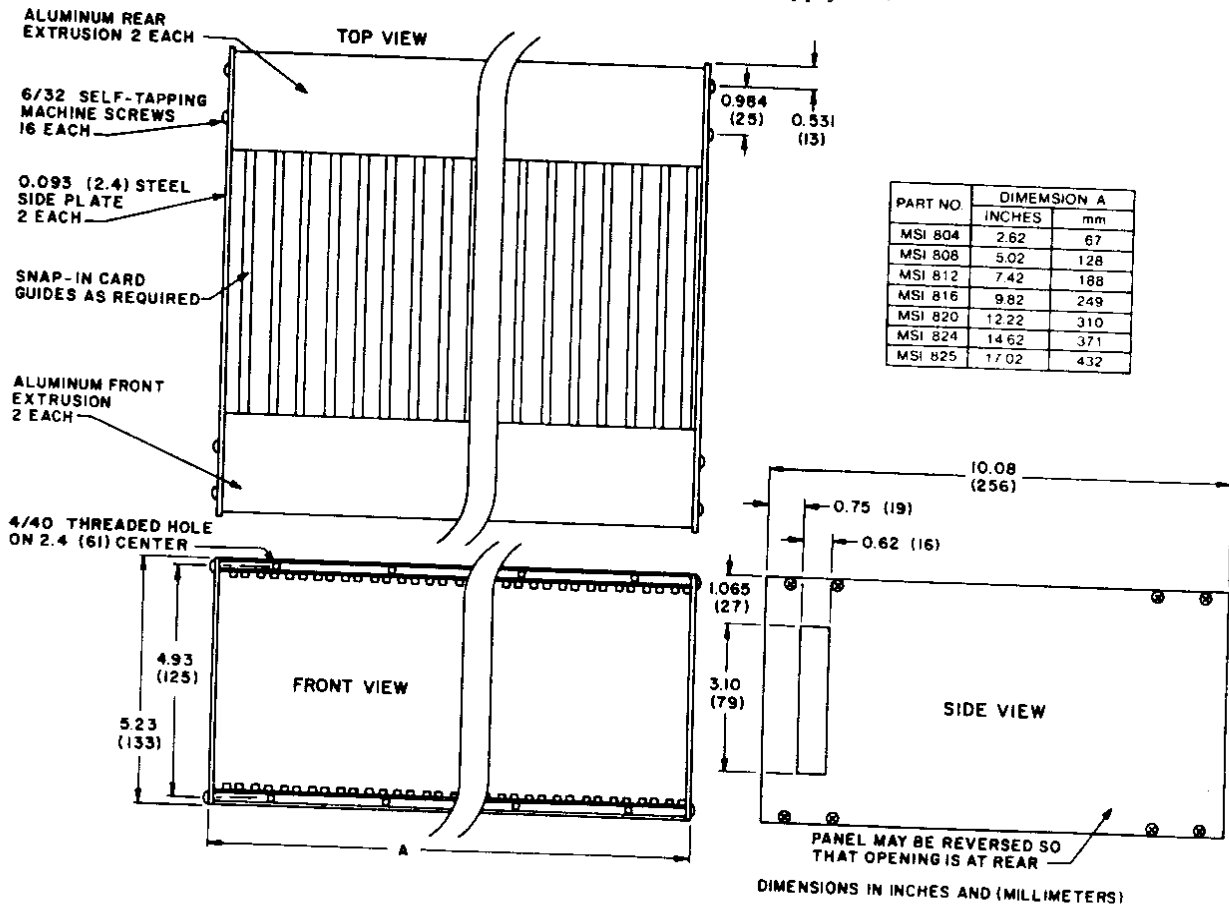


Fig. 1 — Standard chassis MSI 800 series dimensions.

With Flexibility

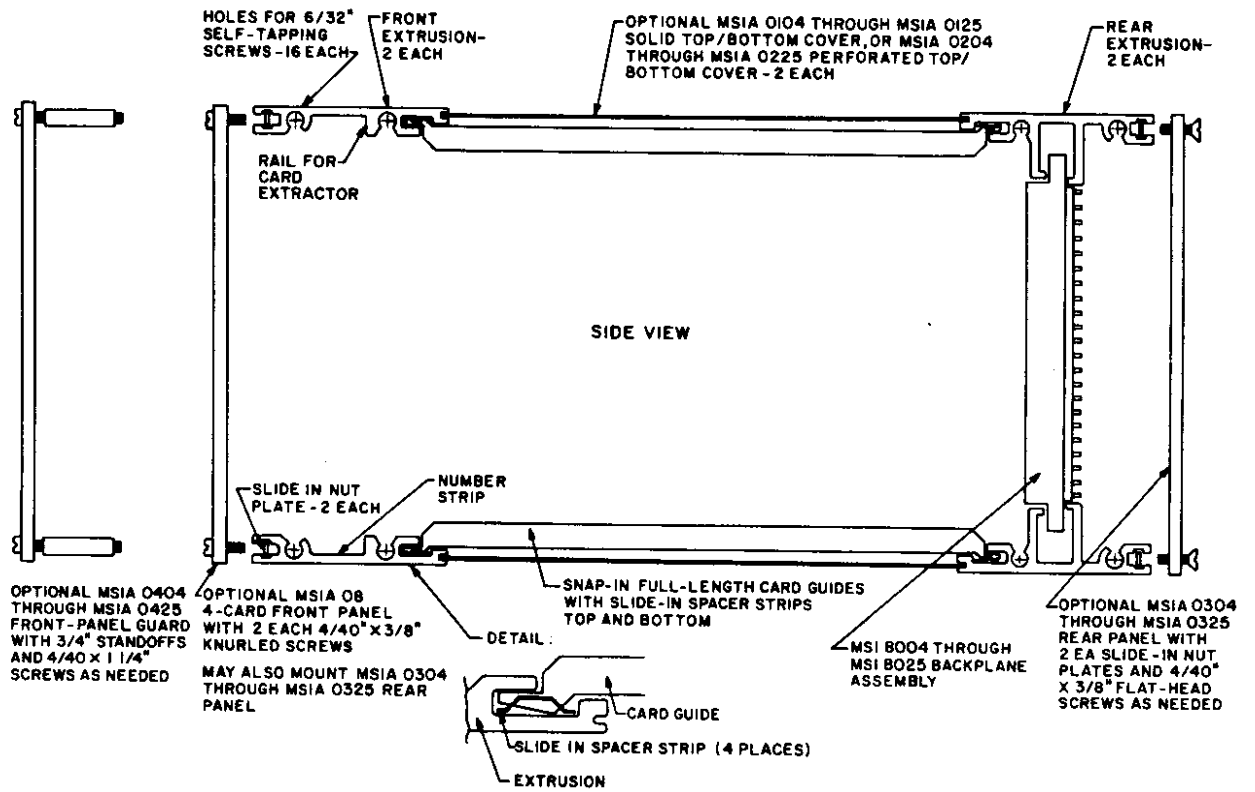


Fig. 2 - Standard chassis MSI 800 series assembly cutaway.

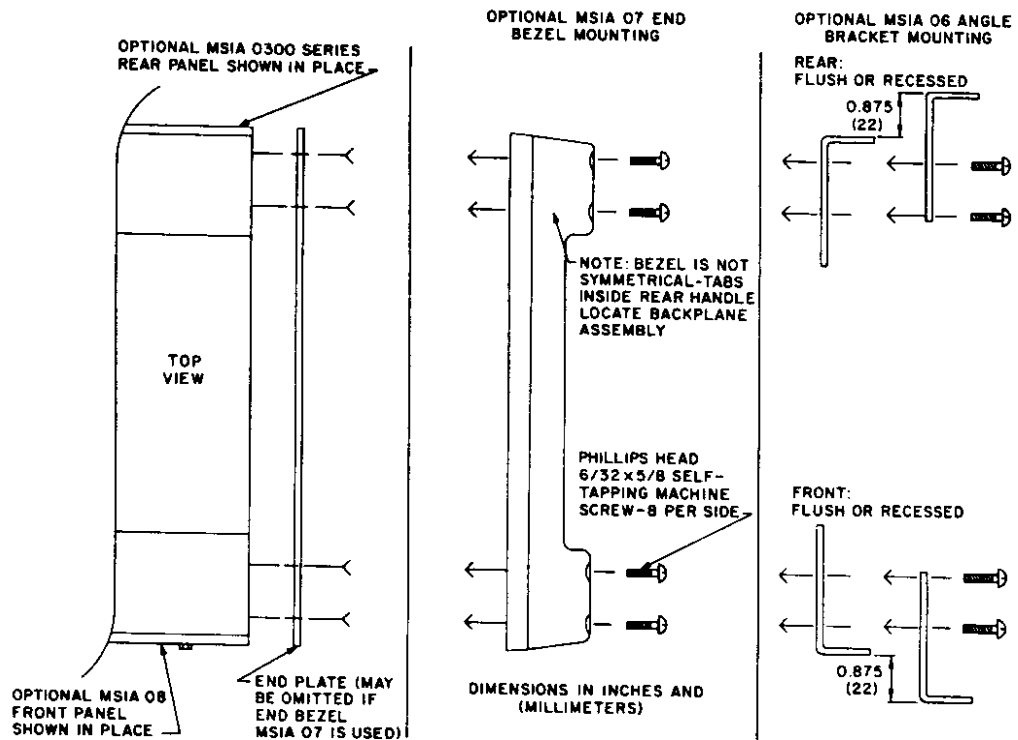


Fig. 3 - Standard chassis MSI 800 series optional end assembly.

MSI 8800 Series Deluxe Chassis

The MSI 8800 series deluxe chassis have full covers and a variety of mounting options added to the standard MSI 800 series. The MSI 8800 series comes assembled with slide-in solid top and bottom covers, screw-fastened front and rear panels, a standoff mounted see-through front panel guard, and two carrying handle/end bezels. Photo D shows an MSI 8825 setup for desk-top use. See Fig. 4 for dimensions, and Table IV for a listing of accessories supplied with the MSI 8800 series.

Two mounting angle brackets are included (loose) to allow flush or recessed mounting from the front or the rear of the chassis. The MSI 8825 may be mounted in a 5-1/4-inch opening of a 19-inch rack and may have either the chassis front or the protective wiring cover flush with the rack front. As in the MSI 800 series,

rubber feet and a power-supply connector are supplied loose. See the discussion under accessories for removal of standoffs from Microboard modules.

Both the end bezels and steel side plates may be left in place, or one or the other may be omitted. With only the end bezels in place, the chassis becomes a good basis for a desk-top development system. The left-most position might mount a CDP18S480 PROM Programmer or CDP18S640 Control and Display Module. See photos E and N. Access to the right-most socket solder side would be useful for board development. Note that for the MSI 8825, the right-most socket is only for power supply use and will not operate Microboards.

The front panel guard supplied is one unit width (2.4-inch) smaller than the chassis width. This space is to provide access to the supply power switch (if used). The MSI-8804 is not supplied with a front panel guard. Guards of any unit width may be bought as options.

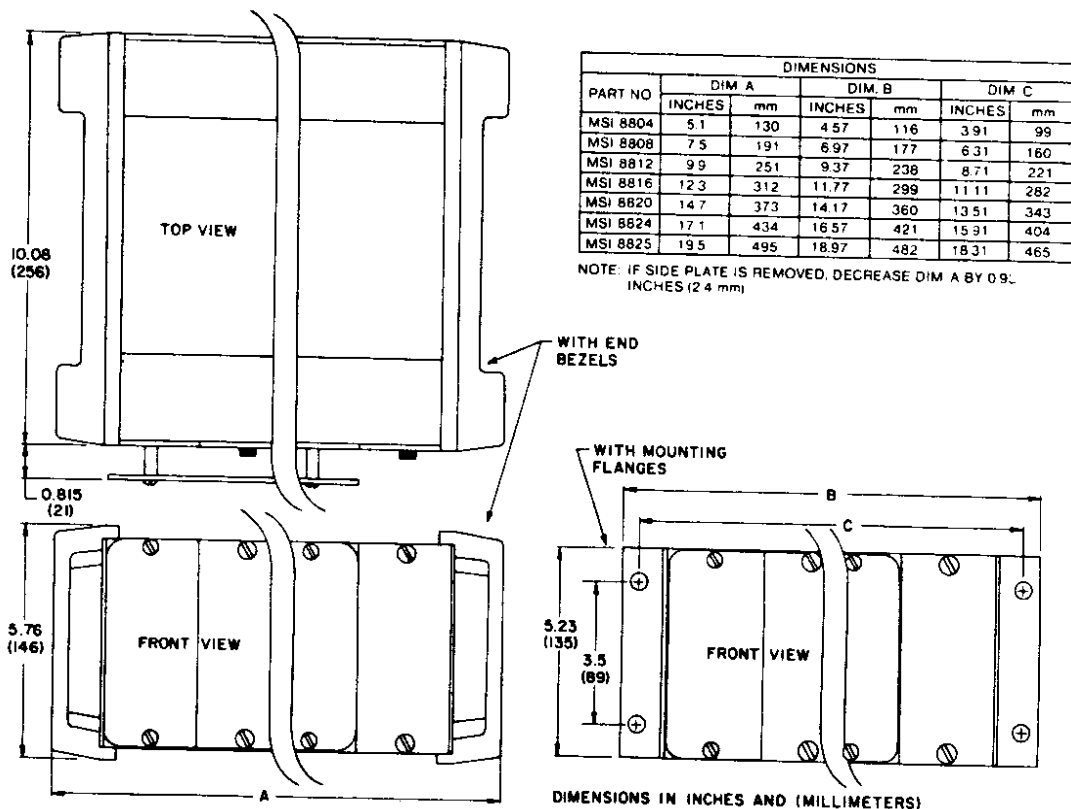


Fig. 4 — Deluxe chassis MSI 8800 series dimensions.

Simple and Economical

MSI 8000 Series: Backplane With Connectors

Each of the MSI 8000 series chassis consists of a backplane (See photo G) with 44-pin, 0.156-inch pitch card edge connectors on 0.6-inch centers. All pins having the same designations are bussed together. Pins 22 and Z (Microboard ground) and 21 and Y (+5 volt) are heavily bussed. See Table III for Microboard backplane pin assignments.

A five-hole pattern on 0.156-inch centers is provided at the extreme left side of the backplane for mounting a power-supply connector. Backplane pins 11 (-15 volts), 12 (spare), and 20 (+15 volts), as well as +5 volts and ground, are wired to this location. See Fig. 6 for connector details. The power supply connector is supplied loose.

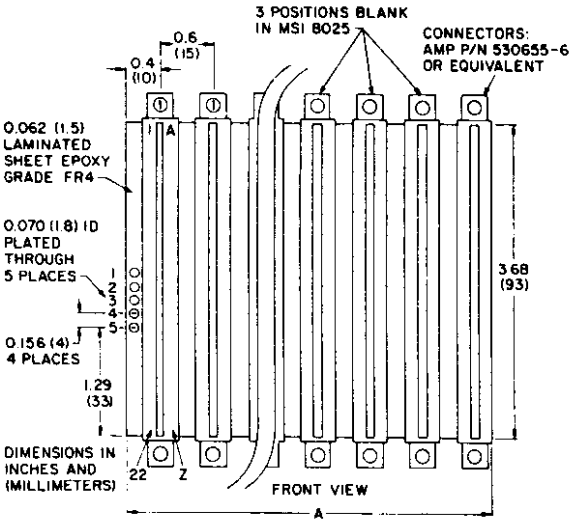
The MSI 8025, 25-card backplane, occupies the same space as a 28-card version would. Connectors 25, 26, and 27 are omitted, however, and the 28th connector is wired only for plug-in power supply connections.

Connector positions are numbered left to right as seen from the connector side, and connector pins are

numbered top to bottom: 1-22 on the left, A-Z on the right. Microboards are to be mounted with components facing left.

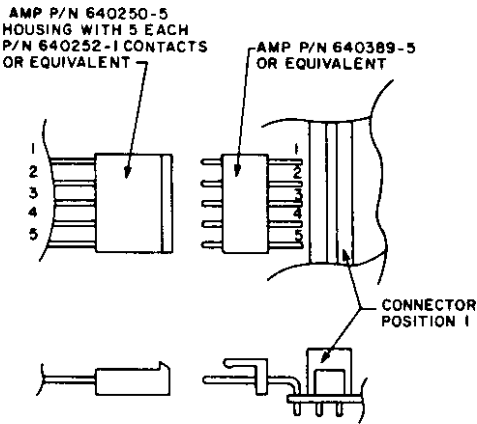
Table III — Microboard Backplane Pin Assignments

Pin	Signal	Pin	Signal
1	DMAI-N	A	TPA-P
2	DMAO-N	B	TPB-P
3	RNU-P	C	DB0-P
4	INT-N	D	DB1-P
5	MRD-N	E	DB2-P
6	Q-P	F	DB3-P
7	SC0-P	H	DB4-P
8	SC1-P	J	DB5-P
9	CLEAR-N	K	DB6-P
10	WAIT-N	L	DB7-P
11	-15 V	M	A0-P
12	SPARE	N	A1-P
13	CLOCK OUT	P	A2-P
14	N0-P	R	A3-P
15	N1-P	S	A4-P
16	N2-P	T	A5-P
17	EF1-N	U	A6-P
18	EF2-N	V	A7-P
19	EF3-N	W	MWR-N
20	+15 V	X	EF4-N
21	+5 V	Y	+5 V
22	GND	Z	GND



PART NO	DIMENSION A	
	INCHES	mm
MSI 8004	2.4	61
MSI 8008	4.8	122
MSI 8012	7.2	183
MSI 8016	9.6	244
MSI 8020	12.0	305
MSI 8024	14.4	366
MSI 8025	16.8	427

Fig. 5 — Backplane MSI 8000 series dimensions.



SUPPLY CONNECTOR PIN NO	BACKPLANE CONNECTOR PIN NO	USE
1	11	-15V
2	12	SPARE
3	20	+15V
4	Y 21	+5V
5	Z 22	GROUND

Fig. 6 — Power supply connector.

MSIA Accessory Series

Table IV lists the accessory part numbers versus the chassis that they fit. Parts that are standard on the Deluxe MSI 8800 series are marked "S"; those that are available optionally to fit are marked "O". Any part marked "S" or "O" will also fit the corresponding Standard MSI 800 series chassis. Table V gives condensed description of each accessory. Accessories are normally supplied in quantities of 10.

MSIA 0100 series **solid top or bottom covers** or MSIA 0200 series **perforated top or bottom covers** slide into slots in the front and rear extrusion (See Fig. 2). To mount the cover one end bezel and/or slide plate must be removed. Only one end plate should be removed at one time and the chassis should not be stressed when the end plate is off.

Note that MSI 0400 series **front panel guards** are normally supplied one size smaller than the corresponding chassis (except MSI 8804), but may be used at any size up to the width of the chassis.

The MSIA 0300 series of **rear panels** can be mounted on the front to replace one or more MSIA08 front panels. An access slot for front entry of cables is thus provided. When a MSIA 0300 series panel is mounted in the rear of a MSI 800 series chassis, a side panel must be removed to insert top and bottom slide-in nut plates supplied with the panel.

The MSIA 10 **cable conduit** is a 19-inch rack mount wiring guide that occupies 1-3/4 inches of rack space.

It has a snap-off aluminum cover and is recessed so that the cover is flush with the rack front. See photo K. It may be used with a MSI 8825 or MSI 825 chassis with angle brackets to guide wiring to the front surface of the chassis. The chassis should be mounted in the recessed position.

Depending on the date of manufacture, Microboards may be equipped with **standoffs**. These standoffs are unnecessary for Microboards installed in the Industrial Chassis Series and should be removed because they may not clear the full-length card guides. If the spacer is a drive pin inside a nylon sleeve, heat the head of the pin for several seconds with a hot soldering iron, and remove the sleeve with pliers. The pin is then free to drop out. Do not use cutters on the pins: they are hardened and will damage cutters or fly apart suddenly.

The MSIA 11 **card extractor** consists of an ejector cam and a snap-on retaining ring. This card extractor is to be inserted through the hole at the top corner of a Microboard and the retaining ring snapped over its pin. The ring is marked "up" for the side away from the board. The ejector cam may be mounted on the bottom corner of the Microboard if the top is not clear, but extra care may be needed to remove and insert the Microboard. The card extractor mounts in a 0.1-inch hole that is 0.15 inch from both the end and the side of the Microboard.

Figs. 7 through 14 give the dimensions for the optional accessories.

Table IV — Accessory Table — MSI 8800 Series.

Chassis	Front Panel MSIA* 08		Front Panel Guard MSIA 04*					Angle Brackets MSIA 06, N=2	End Bezel MSIA 07, N=2	Rear Panel MSIA 03*							
	04	08	04	08	12	16	20			24	25	04	08	12	16	20	24
MSI 8804	S, N = 1		O														
MSI 8808	S, N = 2		S	O				S	S	S							
MSI 8812	S, N = 3		O	S	O			S	S	O	S						
MSI 8816	S, N = 4		O	O	S	O		S	S	O	O	S					
MSI 8820	S, N = 5		O	O	O	S	O	S	S	O	O	O	S				
MSI 8824	S, N = 6		O	O	O	O	S	O	S	O	O	O	O	S			
MSI 8825	S, N = 7		O	O	O	O	O	S	S	O	O	O	O	O	S		
Chassis	Solid Top/Bottom Cover MSIA 01*						Perforated Top/Bottom Cover MSIA 02*						Notes: N = (): Number of these accessories supplied, otherwise N = 1 S = Standard O = Optional — any rear panel MSIA 0300 series marked S or O will fit on front of chassis.				
	04	08	12	16	20	24	25	04	08	12	16	20		24	25		
MSI 8804	S							O									
MSI 8808		S							O								
MSI 8812			S							O							
MSI 8816				S							O						
MSI 8820					S							O					
MSI 8824						S							O				
MSI 8825							S							O			

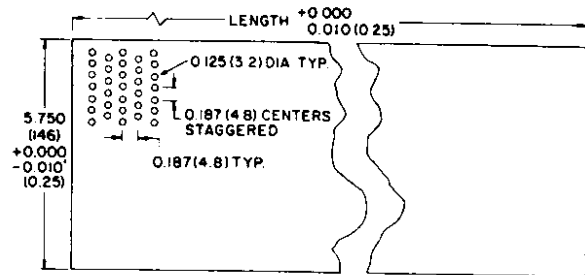
*The last two digits of these designations are one of 04, 08, 12, 16, 20, 24, or 25 depending on size.

For Versatility

Table V — Condensed Description of Accessories for RCA COSMAC Microboard Industrial Chassis Series. See Photos F and K for accessory photographs.

Part Designation	Name	Material	Finish	Fig. No.
MSIA 0100*	Solid Cover (Top or Bottom)	Aluminum	Yellow-Bronze Alodine (inside) Black Paint (outside)	7
MSIA 0200*	Perforated Cover	Aluminum	Yellow-Bronze Alodine (inside) Black Paint (outside)	7
MSIA 0300*	Rear Panel	Aluminum	Yellow-Bronze Alodine	8
MSIA 0400*	Front Panel Guard	Plastic	Gray Transparent	9
MSIA 06	Angle Bracket	Steel	Black Paint	10
MSIA 07	End/Bezel/Handle	Plastic (non-conductive)	Black Paint	11
MSIA 08	Front Panel (4 card)	Aluminum	Yellow-Bronze Alodine	12
MSIA 10	Cable Conduit: Cover Duct	Aluminum Plastic	Yellow-Bronze Alodine Dark Gray	13
MSIA 11	End Brackets Card Extractor	Steel Nylon	Black Paint White	14

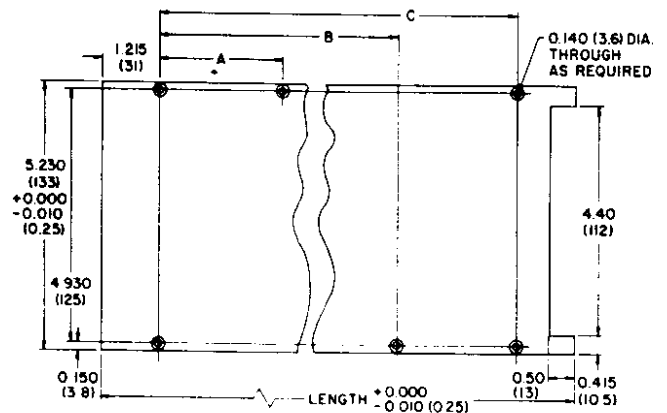
*The last two digits of these designations are one of 04, 08, 12, 16, 20, 24, or 25 depending on size.



HOLE DETAIL FOR MSIA 0200 SERIES PERFORATED COVERS ONLY
DIMENSIONS IN INCHES AND (MILLIMETERS)
MATERIAL: 0.062 (1.6) ALUMINUM
FINISH: INSIDE: ALODINE TREATMENT
OUTSIDE: BLACK TEXTURED PAINT

LENGTH	PART NUMBER	
	SOLID	PERFORATED
2.430 (62)	MSIA 0104	MSIA 0204
4.830 (123)	MSIA 0108	MSIA 0208
7.230 (184)	MSIA 0112	MSIA 0212
9.630 (245)	MSIA 0116	MSIA 0216
12.030 (306)	MSIA 0120	MSIA 0220
14.430 (367)	MSIA 0124	MSIA 0224
16.830 (427)	MSIA 0125	MSIA 0225

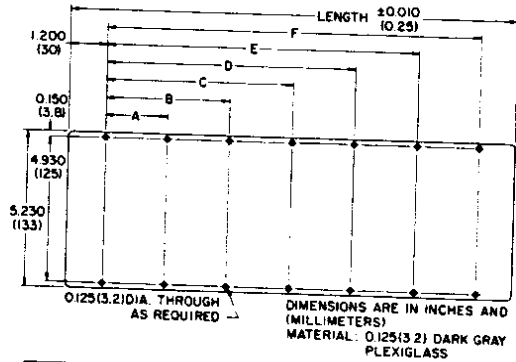
Fig. 7 — MSIA 0100, MSIA 0200 series solid or perforated top and bottom covers.



DIMENSIONS IN INCHES AND (MILLIMETERS)
MATERIAL: 0.125 (3.2) ALUMINUM
FINISH: ALODINE TREATMENT

LENGTH	A DIM	B DIM	C DIM	HOLES REQUIRED	PART NO
2.430 (62)				2	MSIA 0304
4.830 (123)			2.400 (61)	4	MSIA 0308
7.230 (184)			4.800 (122)	4	MSIA 0312
9.630 (245)			7.200 (183)	4	MSIA 0316
12.030 (306)	4.800 (122)	4.800 (122)	9.600 (244)	6	MSIA 0320
14.430 (367)	4.800 (122)	7.200 (183)	12.000 (305)	6	MSIA 0324
16.830 (427)	7.200 (183)	7.200 (183)	14.400 (366)	6	MSIA 0325

Fig. 8 — MSIA 0300 series rear panels.



A	B	C	D	E	F	LENGTH	PART NO.
—	—	—	—	—	—	2.400	MSIA 0404
2.400	—	—	—	—	—	4.800	MSIA 0408
2.400	4.800	—	—	—	—	7.200	MSIA 0412
2.400	4.800	7.200	—	—	—	9.600	MSIA 0416
2.400	4.800	7.200	9.600	—	—	12.000	MSIA 0420
2.400	4.800	7.200	9.600	12.000	—	14.400	MSIA 0424
2.400	4.800	7.200	9.600	12.000	14.400	16.800	MSIA 0425

CONVERSION OF INCHES TO MILLIMETERS:
 2.400 (61); 4.800 (122); 7.200 (183); 9.600 (244);
 12.000 (305); 14.400 (366); 16.800 (427)

Fig. 9 — MSIA 0400 series front panel guards.

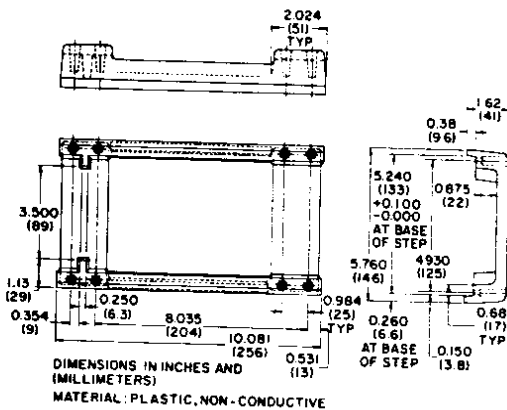


Fig. 11 — MSIA 07 end bezels.

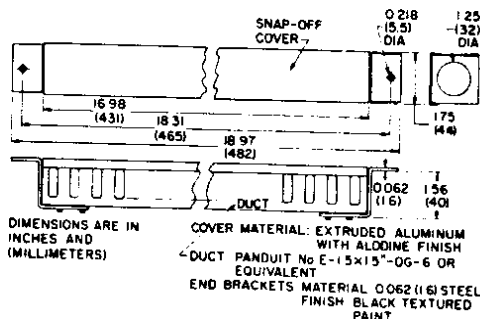


Fig. 13 — MSIA 10 cable conduit.

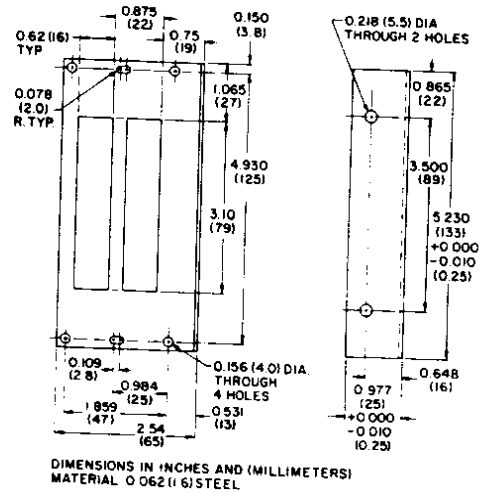


Fig. 10 — MSIA 06 mounting angle brackets.

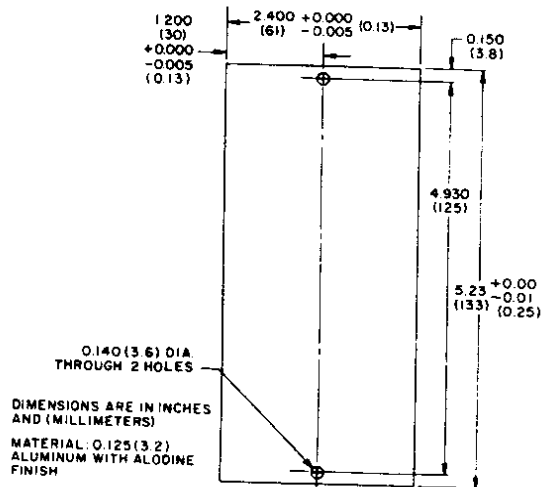


Fig. 12 — MSIA 08 4-card front panel.

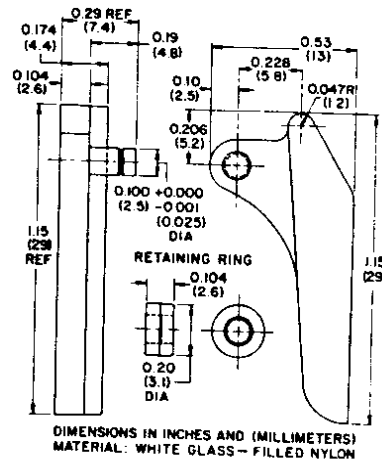


Fig. 14 — MSIA 11 card extractor.

Customer-Selectable Configurations

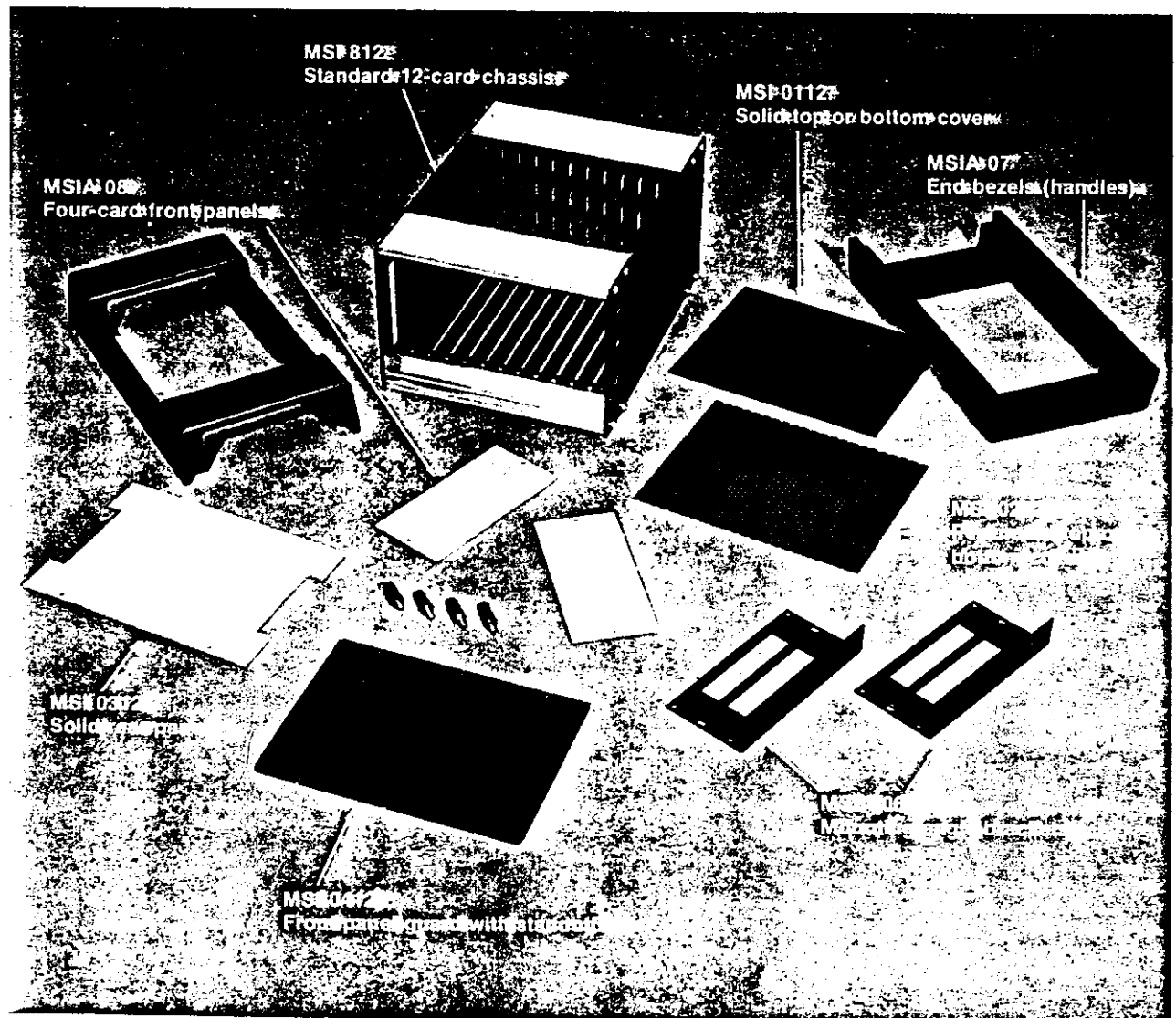


Photo F — Standard 12-card chassis MSI 812 with available accessories identified with call outs.

Optional Plug-In Modules

The RCA Microboard I/O Module Card MSIM 20 mounts in a 4-slot segment of the Industrial Chassis Series and has a mating 4-slot cover with barrier strips for making power connections. The card mounts up to 8 industry standard optically isolated power modules in any mix of AC or DC, input or output signals. LED's mounted on the front panel provide a visual indication of channel activity.

The RCA Industrial Microboard Power Supplies MSIM 40 and MSIM 40E are self-contained front-access switching supplies that plug into any RCA Industrial Series Chassis. They occupy 4 card slots and are complete with power cord, circuit breaker, switch, and power-on light. Operate with either 110 or 220 volts AC and provide logic (5 volts) and analog (+/-15 volts) voltages. They feature a power-down circuit for detecting impending power supply loss.

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RCA Microboard Industrial Chassis Series

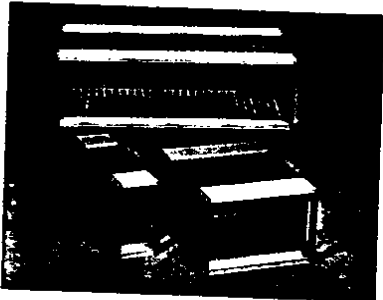


Photo G — Three representative standard chassis. Shown are MSI 825, MSI 812, and MSI 804.

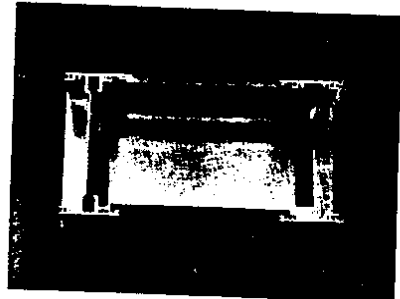


Photo L — Interior of standard 4-card chassis MSI 804. Left side panel is removed to display interior card guides and backplane.

Photo H — MSI 8000 series of backplanes and connectors. Shown are MSI 8004, MSI 8008, MSI 8012, MSI 8016, MSI 8020, MSI 8024, and MSI 8025.

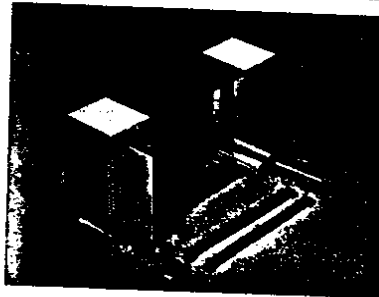
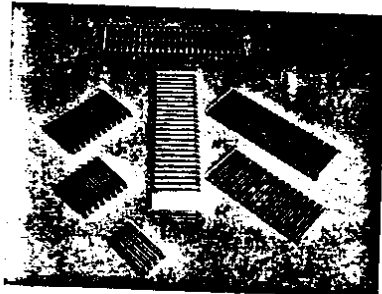


Photo M — Standard 4-card chassis MSI 804 disassembled to show relationship of parts.

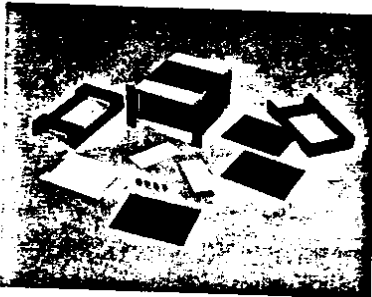


Photo I — Standard 12-card chassis MSI 812 with optional mounting angle brackets in place for flush mounting. Other optional accessories shown are the solid and perforated top and bottom covers, a solid rear panel, a front panel guard with 4 standoffs, and two end bezels (handles).

Photo N — Standard 16-card chassis MSI 816 in typical desk-top configuration. Optional end bezels are added and left side panel is removed to provide access to PROM Programmer module in end position.

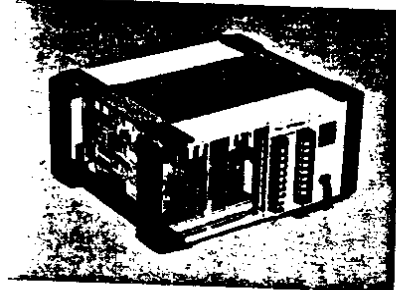


Photo J — Standard 12-card chassis MSI 812 with slotted side panels removed and optional end bezels mounted in place. Optional front panel guard with standoffs, solid and perforated top and bottom covers, and mounting angle brackets are shown unmounted.

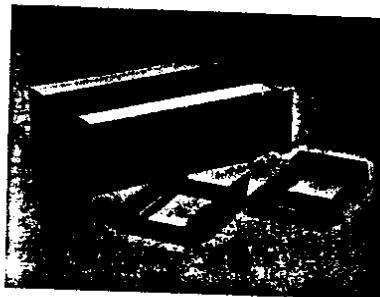
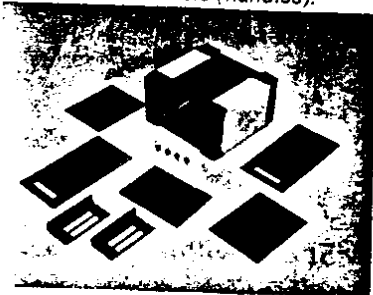


Photo O — Deluxe 25-card chassis MSI 8825 showing all supplied components.

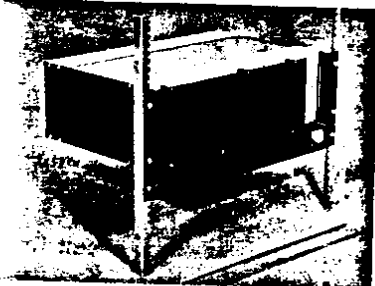
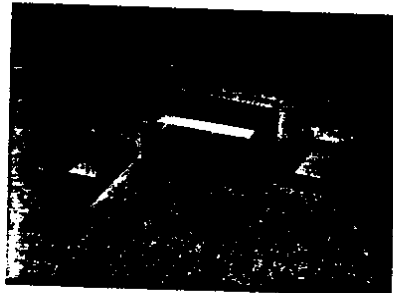


Photo K — Deluxe 25-card chassis MSI 8825 and cable conduit MSI A 10 removed mounted on simulated 19-inch rack.

Photo P — Deluxe 16-card chassis MSI 8816 showing all supplied components.



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PRELIMINARY
**2K x 8 ZEROPOWER™ RAM
MK48Z02 (B) -15/20/25**
FEATURES

- Data retention in the absence of power
- Data security provided by automatic write protection during power failure
- Direct replacement for volatile 2K x 8 Byte Wide Static RAM
- +5 Volt only Read/Write
- Unlimited write cycles
- CMOS - 440 MW active; 5.5 MW standby
- 24-Pin Dual in Line package, JEDEC pinout
- Read cycle time equals write cycle time
- High performance

Part No.	Access Time	R/W Cycle Time
MK48Z02-25	250 nsec	250 nsec
MK48Z02-20	200 nsec	200 nsec
MK48Z02-15	150 nsec	150 nsec

DESCRIPTION

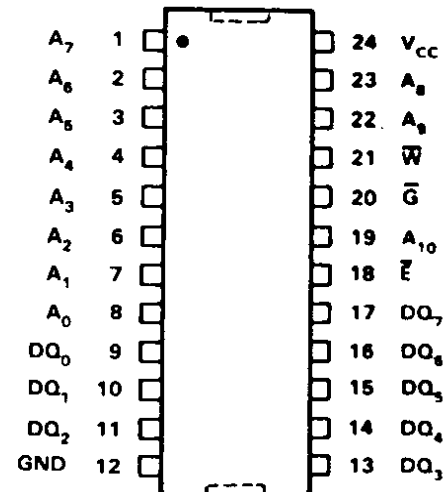
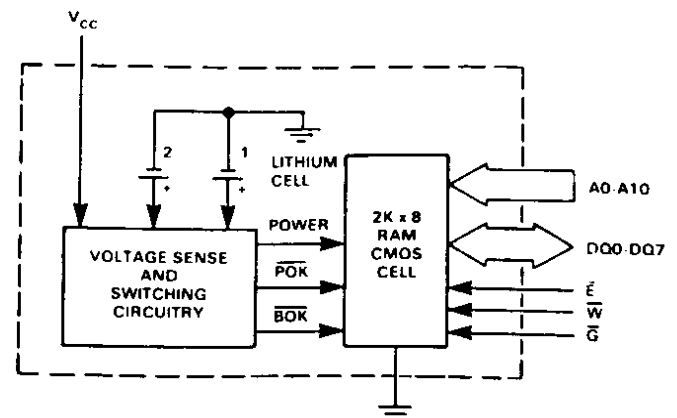
The MK48Z02 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using HCMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has all the sought-after characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Extraordinary low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted

TRUTH TABLE

V _{CC}	\bar{E}	\bar{G}	\bar{W}	MODE	DQ	POWER
≤5.5 volts	V _{IH}	X	X	Deselect	High Z	Standby
	V _{IL}	X	V _{IL}	Write	D _{IN}	Active
≥4.75 volts	V _{IL}	V _{IL}	V _{IH}	Read	D _{OUT}	Active
	V _{IL}	V _{IH}	V _{IH}	Read	High Z	Active
<4.5 volts	X	X	X	Write Protect	High	Zero

PIN NAMES

A ₀ - A ₁₀	Address Inputs	V _{CC}	Power (+5 V)
\bar{E}	Chip Enable	\bar{W}	Write Enable
GND	Ground	\bar{G}	Output Enable
DQ ₀ - DQ ₇ Data In/Data Out			

PIN CONNECTIONS
Figure 1

BLOCK DIAGRAM
Figure 2


CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity during the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02 also matches the pinning of 2716 EPROM and 2K x 8 E²PROM. Like other static RAM, there is no limit on the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require +5 volts only, no additional support circuitry is needed to interface to a microprocessor.

OPERATION

Read Mode

The MK48Z02 is in the Read Mode whenever \overline{W} (Write Enable) is high and \overline{E} (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2048 bytes of data is to be accessed.

Valid data will be available to the eight Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the \overline{E} and \overline{G} (Output Enable) access times are satisfied. If \overline{E} or \overline{G} access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the eight Data I/O signals is controlled by the \overline{E} and \overline{G} control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA} , but the data lines will always have valid data at t_{AA} .

Write Mode

The MK48Z02 is in the Write Mode whenever the \overline{W} and \overline{E} inputs are in the low state. The latter occurring falling edge of either \overline{W} or \overline{E} will determine the start of the Write Cycle. Therefore, t_{AS} , t_{WD} , and t_{CEW} are referenced to the latter occurring edge of \overline{E} or \overline{W} . The Write Cycle is terminated by the earlier rising edge of \overline{E} or \overline{W} . The addresses must be held valid throughout the cycle. \overline{W} must return to the high state for a minimum of t_{WR} prior to the initiation of another cycle.

If the output bus has been enabled (\overline{E} and \overline{G} low), then \overline{W} will disable the outputs in t_{WEZ} from its falling edge; however, care must be taken to avoid a potential bus contention. Data-In must be valid t_{DS} prior to the rising edge of \overline{E} or \overline{W} and must remain valid for t_{DH} after the rising edge of \overline{E} or \overline{W} .

Data Retention Mode

The ZEROPOWER RAM provides full functional capability for V_{CC} above 4.75 volts, guarantees write protection for V_{CC} less than 4.50 volts, maintains data in the absence of V_{CC} , and needs no additional support circuitry. The block diagram shown in Figure 7 illustrates this self-contained solution.

The MK48Z02 constantly monitors V_{CC} . Should the supply voltage decay, the RAM will automatically write-protect itself in the V_{CC} range between 4.75 and 4.50 volts (Figure 6). Once V_{CC} falls below 4.50 volts, all inputs to the RAM become "DON'T CARE" ($-0.3 \leq V_{IN} \leq 5.5$ volts), and all outputs are high impedance.

As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects one of two Lithium cells that supply the power necessary to retain data. A decision as to which cell to use is made on the basis of highest voltage. The redundant Lithium cells are independent rather than parallel, to enhance reliability. (Furthermore, each cell comes from a different manufacturing lot). In the data retention mode, junction leakage (I_L) is the only current requirement. Leakage, typically 300 pA, is supplied from a Lithium cell.

During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the Lithium cell. As V_{CC} rises from 4.50 to 4.75 volts, the Lithium cells are checked; if the voltage in either cell is below 2.0 V, a flag will be set. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts. The flag can be checked on the first write cycle after a power-up. This first write cycle will not be executed if either Lithium cell has been depleted, thereby warning of an impending data loss.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.3 V to +7.0 V
Operating Temperature T_A (Ambient)	0°C to +70°C
Storage Temperature (Ambient)	-20°C to +70°C
Power Dissipation	1 Watt
Output Current	20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below -0.3 V DC.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	$V_{CC} + 0.5 V$	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,6

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) ($V_{CC} = 5.0 \text{ volts} \pm 10\% - 5\%$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	5
I_{CC2}	TTL Standby Current ($\bar{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\bar{E} \geq V_{CC} - 0.2 V$)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	-1	+1	μA	2
I_{OL}	Output Leakage Current	-5	+5	μA	2
V_{OH}	Output Logic "1" Voltage ($I_{OUT} = -1.0 \text{ mA}$)	2.4		V	
V_{OL}	Output Logic "0" Voltage ($I_{OUT} = 2.1 \text{ mA}$)		0.4	V	

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) ($V_{CC} = 5.0 V \pm 10\% - 5\%$)

SYM	PARAMETER	MK48Z02-15		MK48Z02-20		MK48Z02-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	3
t_{CEA}	Chip Enable Access Time		150		200		250	ns	3
t_{CEZ}	Chip Enable Data Off Time		35		40		50	ns	
t_{OEA}	Output Enable Access Time		55		65		75	ns	3
t_{OEZ}	Output Enable Data Off Time		35		40		50	ns	

AC ELECTRICAL CHARACTERISTICS (Cont.)

($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$) ($V_{CC} = 5.0\text{V} + 10\% - 5\%$)

SYM	PARAMETER	MK48Z02-15		MK48Z02-20		MK48Z02-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{OH}	Output Hold from Address Change	15		15		15		ns	
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{WD}	Write Pulse Width	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{WEZ}	Write Enable Data Off Time		50		60		80	ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

CAPACITANCE ($T_A = 25^{\circ}\text{C}$)

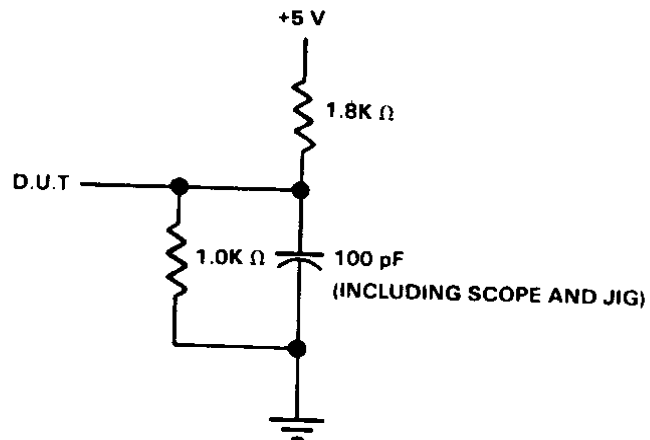
SYM	PARAMETER	MAX	NOTES
C_1	Capacitance on all pins (except D/Q)	7 pF	9
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,9

NOTES:

- All voltages referenced to GND.
- Measured with $GND \leq V_1 \leq V_{CC}$ and outputs deselected.
- Measured with load as shown in Figure 3.
- Output buffer is deselected.
- I_{CC1} measured with outputs open.
- Negative spikes of -1.0 volts allowed for up to 10 ns once per cycle.
- See MK48Z02 Reliability Report for statistical data on accelerated operational life studies and methods of predicting data retention time t_{DR} .
- Each MK48Z02 is marked with a 4 digit data code XXYY, XX designates the year of manufacture and YY designates the week in that year. Example 8340 would be interpreted as year 1983 week 40 or September 25, 1983. The expected t_{DR} is defined as starting at date of manufacture and proceeding without interruption.
- Effective capacitance calculated from the equation $C = \frac{\Delta I \cdot t}{\Delta V}$, with $\Delta = 3$ volts and power supply at nominal level.

OUTPUT LOAD DIAGRAM

Figure 3

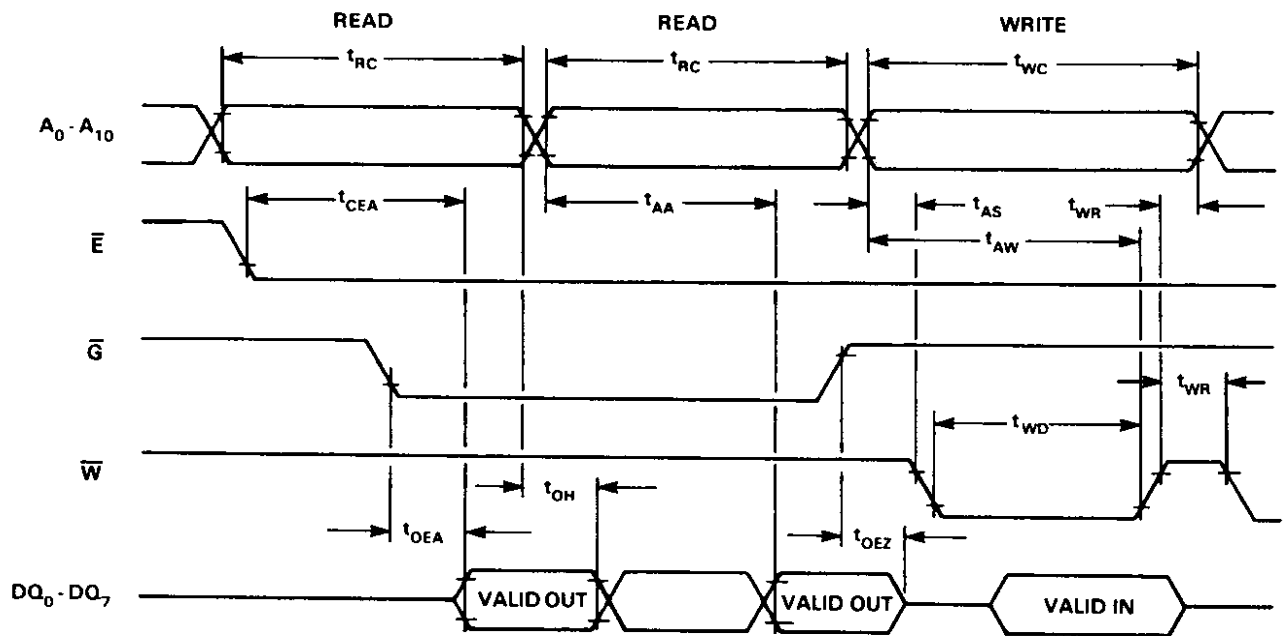


A.C. TEST CONDITIONS

Input Levels: 0.6 V to 2.4 V
 Transition Times: 5 ns
 Input and Output Timing
 Reference Levels: 0.8V or 2.2 V

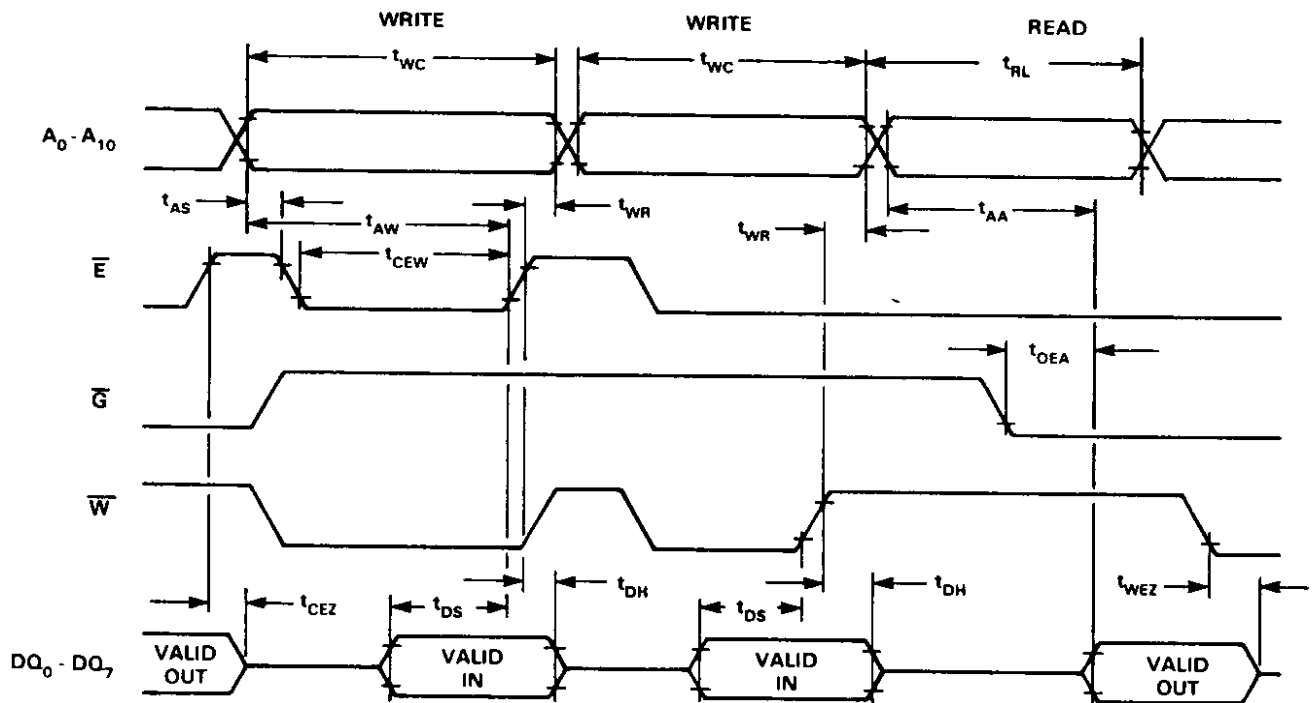
TIMING DIAGRAM

Figure 4



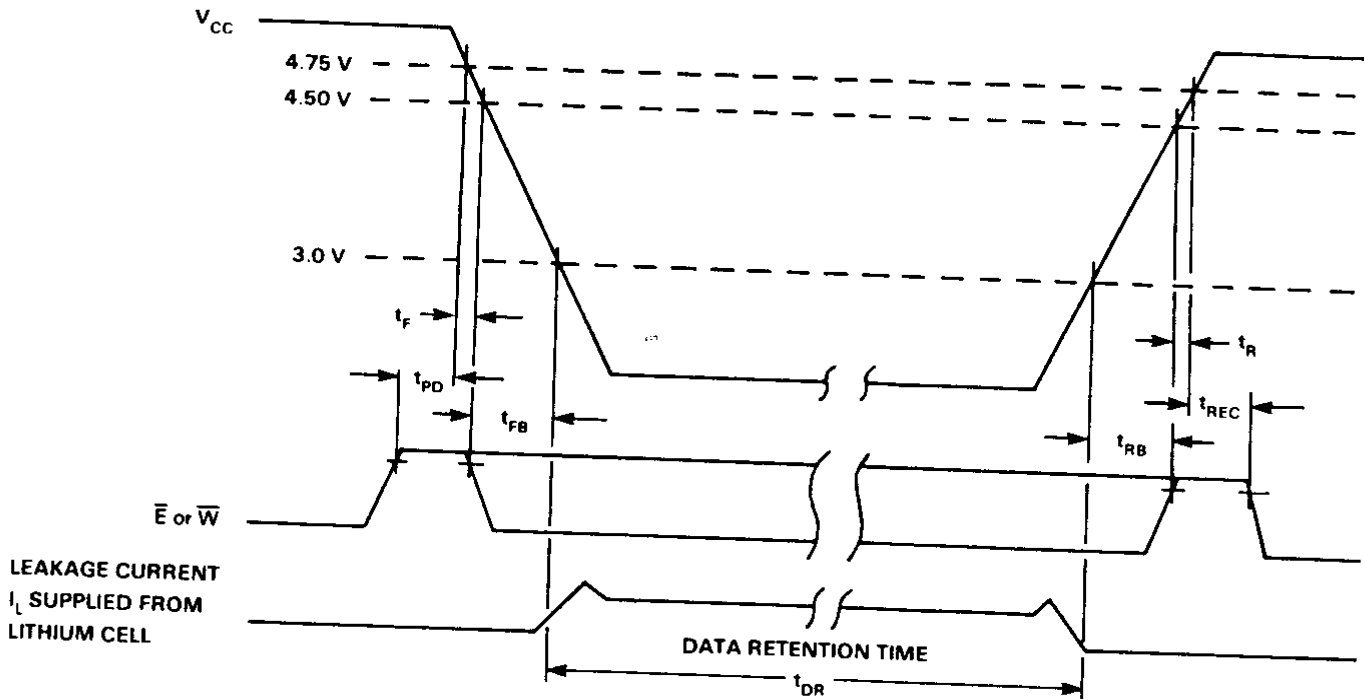
TIMING DIAGRAM

Figure 5



POWER-DOWN, POWER-UP CONDITIONS

Figure 6



POWER-DOWN/POWER-UP TIMING
($0^\circ\text{C} \geq T_A \leq +70^\circ\text{C}$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	\bar{E} or \bar{W} at V_{IH} before Power Down	0		μS	
t_F	V_{CC} slew from 4.75 V to 4.50 V (\bar{E} or \bar{W} at V_{IH})	300		μS	
t_{FB}	V_{CC} slew from 4.50 V to 3.0 V	10		μS	
t_{RB}	V_{CC} slew from 3.0 V to 4.50 V	1		μS	
t_R	V_{CC} slew from 4.50 V to 4.75 V (\bar{E} or \bar{W} at V_{IH})	0		μS	
t_{REC}	\bar{E} or \bar{W} at V_{IH} after Power Up	2		ms	

($T_A = 25^\circ\text{C}$)

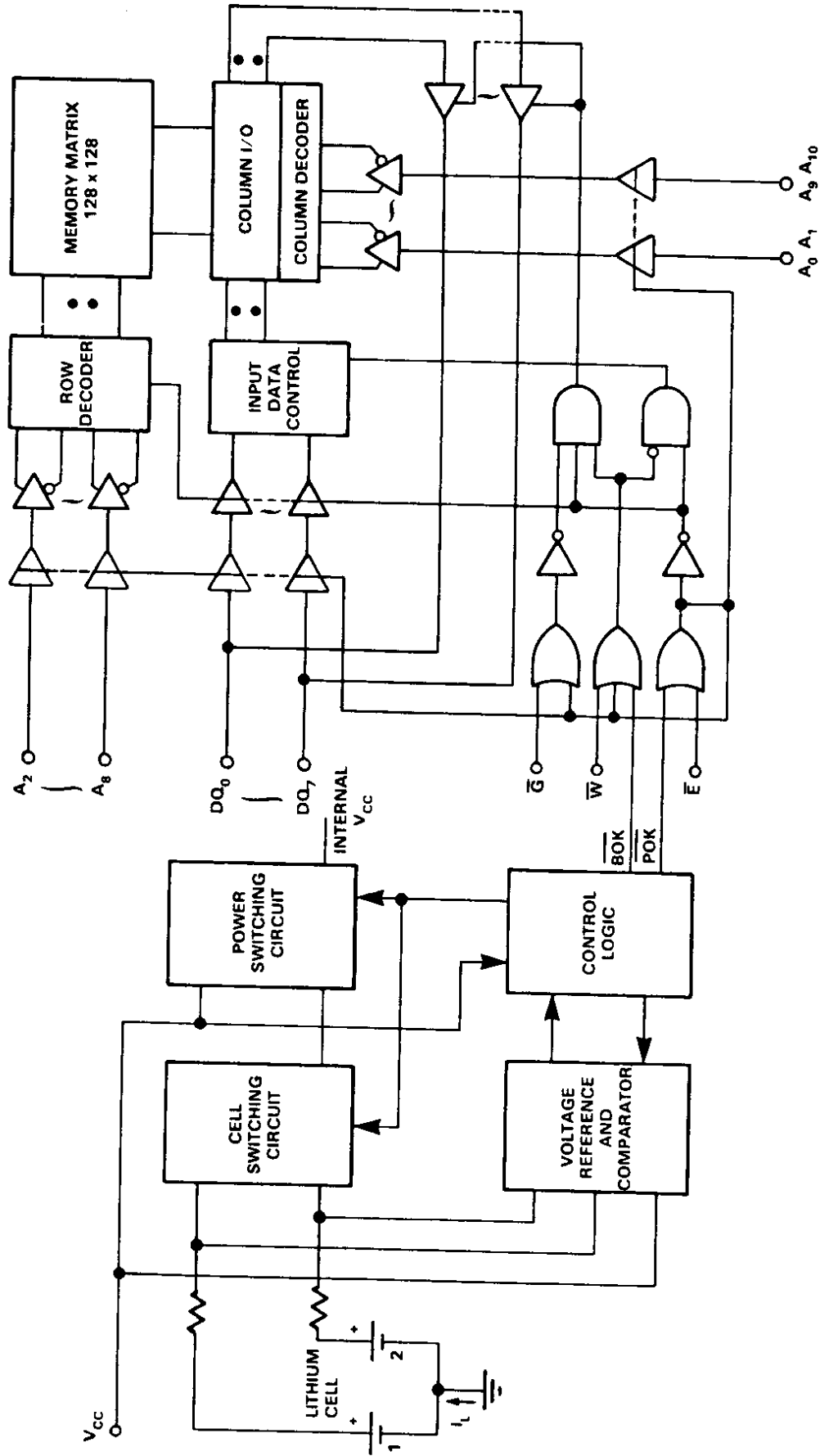
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	7,8

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

ZEROPOWER RAM FUNCTIONAL DIAGRAM

Figure 7

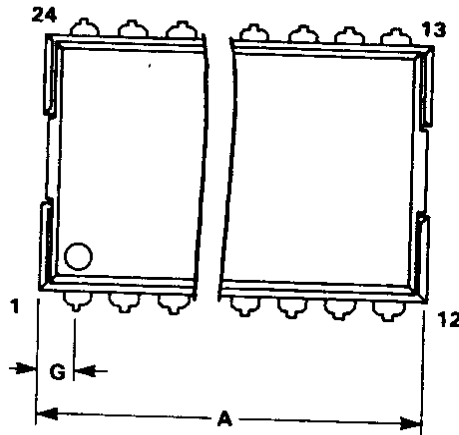


ORDERING INFORMATION

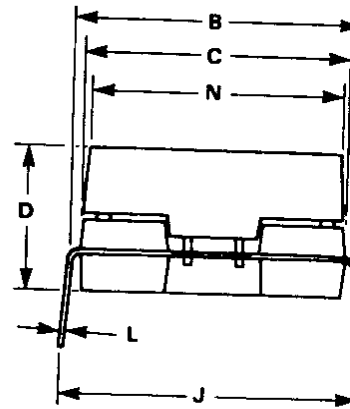
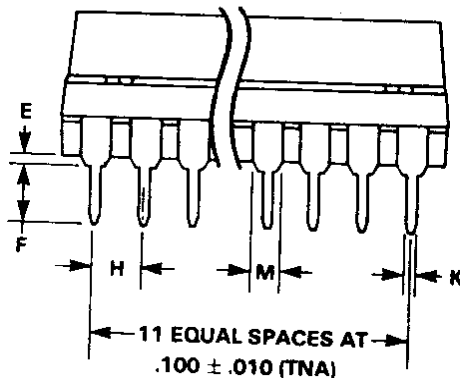
PART NO.	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK48Z02B-15	150 ns	Plastic	0° to 70°C
MK48Z02B-20	200 ns	Plastic	0° to 70°C
MK48Z02B-25	250 ns	Plastic	0° to 70°C

PACKAGE DESCRIPTION

B Package
24 Pin



DIM	INCHES		NOTES
	MIN	MAX	
A	-	1.270	2
B	.530	.540	
C	.530	.550	
D	.300	.320	
E	.015	-	3
F	.120	.180	
G	.080	.090	
H	.090	.110	
J	.800	.700	4
K	.015	.021	5
L	.008	.012	5
M	.045	.070	
N	.550	.570	



NOTES:

- Lead finish is to be specified on the detail specifications.
- Overall length includes .010 in. flash on either end of the package.
- Package standoff to be measured per JEDEC requirements.
- Measured from centerline to centerline at lead tips.
- When the solder lead finish is specified, the maximum limit shall be increased by .003 in.



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270-272 Avenue de Tervuren (BTE21), B-1150 Brussels, Belgium;
Telephone: 762.18.80

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30 to 100 Watt High Performance DC-DC Converters/ *DCS Single, Dual and Triple Outputs.*

APPLICATIONS

Telecommunications
Data Acquisition
Robotics
Remote Systems
Process Control
Battery Operated Systems
Uninterruptable Power Systems
Test Instrumentation
Ground Support Equipment
Commercial and Military

DESIGN FEATURES

WIDE 2:1 INPUT RANGES
INPUT: 9-18VDC, 18-36VDC,
and 36-72VDC

EXTERNAL SYNC: User can externally synchronize the DCS to a system clock. This feature will improve the overall system signal-to-noise ratio as all internal switching of the converter will be "locked" to a system rate. In the event of loss of external sync, the DCS will "free run" on its own internal oscillator.

EXTERNAL DISABLE: Remote TTL turnoff for power conservation. In the "disable" mode the DCS dissipates less than 0.75 watts.

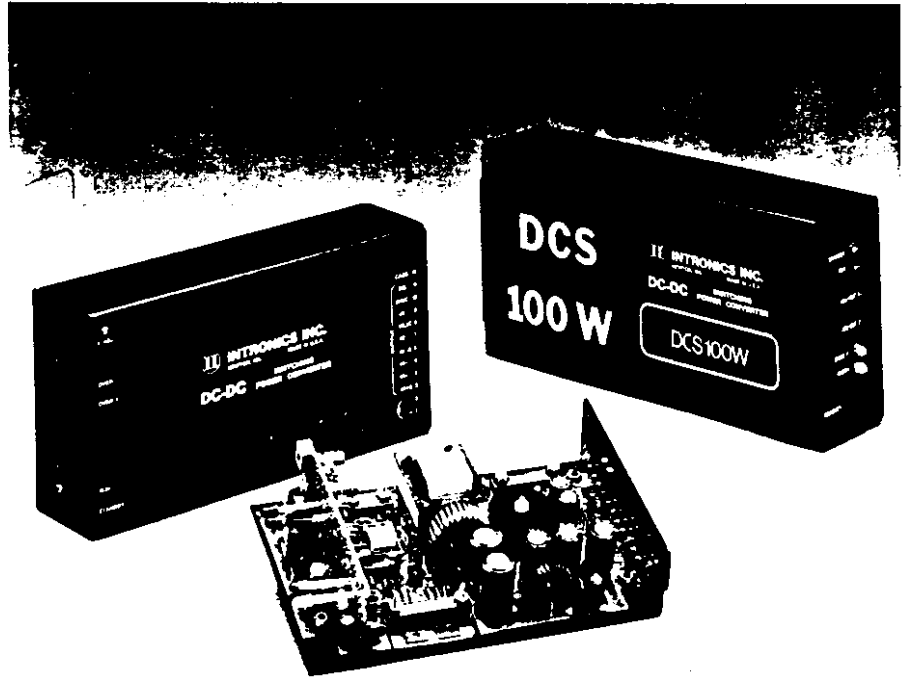
DISPLAY INDICATORS: 4 LED's provide indication of status modes. The indicators can simplify system troubleshooting.

SOFTSTART: Designed to gradually increase the duty cycle of the pulse-width-modulation (PWM) from zero to its normal operating point. This soft-start eliminates voltage transients and limits inrush current during startup.

HIGH EFFICIENCY: Typically 71% (80% max)—which does not vary more than 3% over the full 2:1 input range.

PARALLEL OPERATION: The DCS series may be connected in parallel for increased current capability.

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1616 Bigelow Ave. North
Seattle, WA 98109
(206) 285-2525



POWER DESIGN: All models have been designed to provide up to 80% of full output power from any individual output up to the full power rating of the unit. Not only are nominal ratings shown, but "absolute maximum" is indicated for multiple outputs. The designer is not restricted to the ratings shown but can use the DCS up to maximum indicated in models chart provided that rated "power" is not exceeded.

INPUT TO OUTPUT ISOLATION: 1000VDC Typical.

FULLY REGULATED OUTPUTS: Provision has been made for the derived outputs to be fully regulated. This option improves the line and load regulation by a factor of 10 and virtually eliminates typical cross regulation interaction between the primary and derived outputs.

REMOTE SENSE: Remote sense on the primary output compensates for IR drop of up to 0.5V. Internal sensing is automatic if remote sense lines are either open or shorted.

SHOCK AND VIBRATION: Option available to vibration of up to 5g's.

GENERAL DESCRIPTION

The DCS series is a complete family of DC to DC converters ranging from 30 to 100 Watts of power. There are more than 100 models which are available in single, dual, or triple outputs; and input can be selected from three 2:1 ranges of 9-18VDC, 18-36VDC, or 36-72VDC. Each power rating is available with outputs of +5, -5, +12, +15, +24, +28, ± 12 , ± 15 , and ± 18 VDC.

The DCS series was designed to meet the needs of a design engineer rather than just matching competitive model types currently available. By incorporating features such as external synchronization provision, external disable, display status indicators, semi-regulated and fully regulated outputs, and high efficiency, the DCS series provides the user with a system component far superior to conventional DC to DC converters.

500 P. 6 A 7
AC

DCS Theory of Operation

The DCS series of 30-, 50-, and 100-watt DC-DC converters was first introduced in late 1981. Since its introduction, this series has been expanded and improved upon so that today it offers the Design Engineer a price/performance ratio unmatched in the industry. Many of the 136 different models have been used in applications such as telecommunications, process control, vehicle-mounted instrumentation, and oil exploration — wherever performance, quality, and systems features are required.

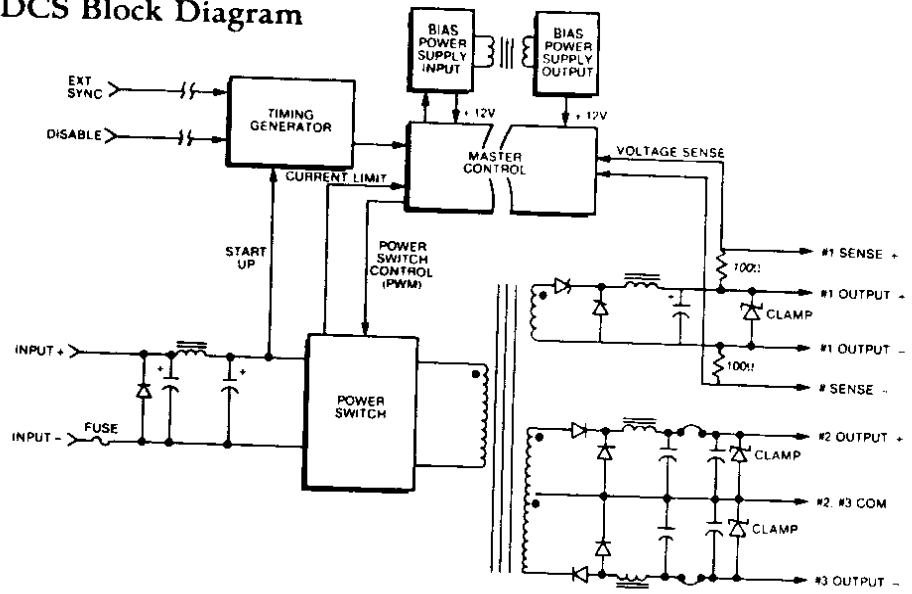
The DCS series utilizes the "forward converter" type of topology as opposed to a "fly-back" scheme due to the inherent lower noise produced on the output.

In a forward converter (see Block Diagram), the transistor switch produces a pulse train whose amplitude varies according to the input line and whose width is modulated by means of a master control to maintain a constant output. This pulse train is fed into the transformer and integrated by the LC filter. The output voltage is sensed and fed back into the master control which varies the "on" time of the power transistor, thereby controlling the amount of power that is fed into the integrator. Although the forward converter comprises the major element in the DCS block diagram as shown, the power train is only a portion of the total power supply. One of the most important parts is what we call the "logic card" which controls an independent bias supply as well as the forward converter.

A master timing generator feeds a clock signal into portions of the logic card, one portion of which controls an independent bias supply. This "power supply" is independent of the main output. It is there solely to provide housekeeping power on both sides of the isolation barrier and to allow for proper operation of all the complex circuits without their having to be dependent upon outside phenomena such as short circuit, overvoltage, turn-on, or turn-off conditions.

There is sufficient reserve in the bias power supply to keep the logic card up for some time after the power for the main power switches ceases to be there. The bias supply is very im-

DCS Block Diagram



portant in that it allows us to do these things without having to affect the main loop. It also provides well-regulated power from which to operate many other functions without becoming a victim of a sloppy internal power supply. In addition, this scheme is more efficient than using a series-pass power supply as a means of maintaining housekeeping power.

The master control of the logic card has an optically isolated error amplifier which uses a high-quality operational amplifier in the temperature compensated precision voltage reference. Similarly, the overvoltage circuit employs an optically isolated, independent error-detection scheme that is not tied to the remote sense lines as are the overvoltage types of protection found on many competitive units. It also does not rely on the same feed-back path as the error amplifier; therefore, if there were something wrong with the error amplifier, the overvoltage has a redundant path to over-ride it and to shut down the supply. This alternate path is only used in the condition of overvoltage; therefore, its components are not subject to any stress, per se, as they are all in an "off" position until the fault occurs.

The output error amplifier has also been designed to provide zero volts on the output in the event of fault. Other design considerations include a disable scheme which is optically isolated through the overvoltage circuit and a sync circuit that is optically isolated from the timing generator.

Disable is referenced to output low, and is connected via the over voltage circuit. The Disable terminal forces the unit into standby status. When a +5 source of $\approx 20\text{mA}$ is applied to that terminal, no limiting is required. When higher voltages are used, please limit current to 20mA. Upon application of the Disable voltage the following sequence of events occurs:

1. $\approx 5\text{ms}$: Terminates output modulation.
2. $\approx 100\text{ms}$: Terminates internal modulation functions.
3. $\approx 500\text{ms}$: Reduces internal current drain, illuminates standby LED.

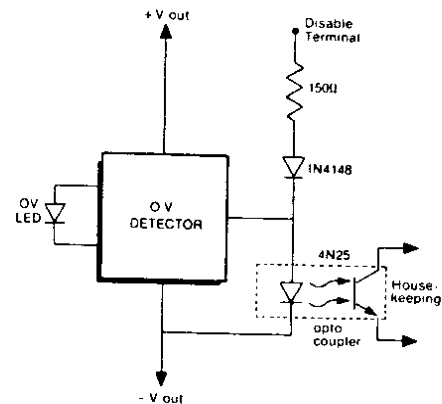


Figure A

The external sync is a port into the timing generator by which a square-wave timing signal can be fed to move the switching frequency of the power converter either plus or minus 10%. This particular feature is unusual in that the converter can be made to move over or under its default frequency. Most synchronization schemes only allow them to move in one direction, usually only up in frequency.

The logic card itself has many fault-detection schemes employed throughout. Conditions such as overload, overvoltage, stand-by, power off, and power on, all initiate a soft-start cycle. In soft-start, the output is increased in a slow controlled fashion, instead of being allowed to rise as fast as it can leading to the possibility of overshoot. Once the output voltage has risen to its near-nominal value, the error amplifier will take control of the output voltage and will maintain it at its preset value.

In the event of a signal requiring the total shutdown of the logic card (in other words, disable) housekeeping functions within the converter are terminated in a sequence-controlled fashion. First, the main power switch is turned off, then the bias supply is turned off, and finally the timing generator is shut off. Even the internal start-up supply, which is a series-pass regulator driven off the input voltage, is shut down so there are no internal housekeeping requirements other than that required to light the LED on the front panel. This allows for very low stand-by currents (In most cases, less than 1/2 watt dissipation).

The DCS Block Diagram shows the derived outputs (outputs 2 & 3) as being windings off the main power transformer fed into separate filter inductors and capacitors. This scheme as shown is known as a "semi-regulated output". It provides good line regulation and a reasonably good load regulation, depending upon the requirement. If you can tolerate a 5-10% deviation in total voltage and can always provide a minimum load of 10% of the nominal rated output of that channel, semi-regulated models can offer distinct cost advantages. For applications where tighter regulation is required, Intronics offers a fully regulated option. The 30 and 50 watt series use a series-pass type regulation scheme while the 100-watt units use a pulse-width-modulation scheme (PWM) to control the derived output voltage. This frees us from the dissipation-limited linear regulators that work well on lower power units. The 100-watt series is available with fully regulated outputs only.

The DCS series is a switching power supply which has a sensing and control network to regulate the outputs to the limits of the specification. Sensing must be done to accomplish this control. To accomplish this, a minimum preload of 10% is required on all outputs. Below this preload condition on the primary output, the terminal derived output voltage(s) of a DCS could be 0VDC. Additionally, the derived output voltage(s) will increase to a clamp limit below a preload condition on the derived outputs (see Figure Ba). Intronics could have installed a preload inside the DCS at the output terminals; however, the trade-off of efficiency for this condition is not in the user's best interest. Without a preload, all outputs will fall outside specified limits.

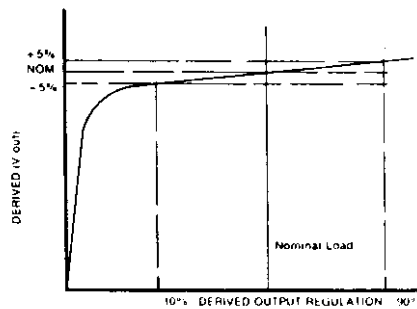


Figure Ba Derived Outputs vs Primary Current

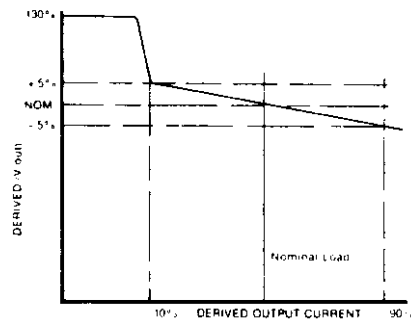
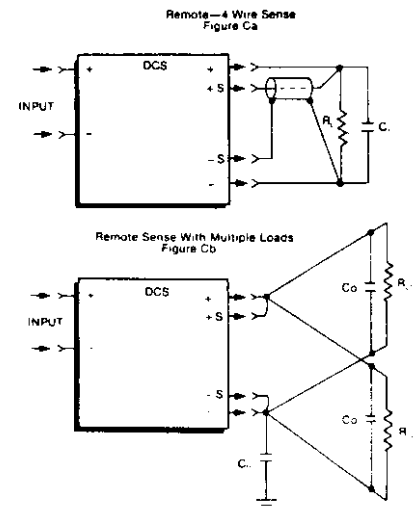


Figure Bb Derived Output vs Derived Current

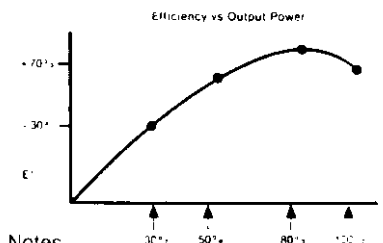
The DCS provides remote sensing for those units having an output loaded in the #1 position; in other words, all singles and triples, and those duals with +5V outputs. Remote sense measures the voltage applied to the load and allows for compensation due to IR drops of up to 10%. Care should be taken, however, that this 10% is not exceeded. Otherwise, there is the risk of tripping the overvoltage circuit which monitors the output pins and is set internally. For example, if the voltage at the load was 5V, the voltage at the supply could be 5.8V which is very near the overvoltage point. It would only require a slight degradation or increase in the load to push the unit to the OV point. You could not get 5.8V @ 10A out, however, because you would trip overcurrent. Output power maximum is power delivered out of the supply not delivered to the load.

Remote or four wire sensing (Figure Ca) provides complete compensation for DC voltage drops in the connecting cables. Power leads should be twisted and run together. Shield sense leads and route for minimum noise pickup. If the positive output is grounded, the negative sense lead should be shielded. If the output is floating, shield both sense leads and connect shield to chassis ground. Capacitor (C₁) is suggested to reduce output impedance and prevent instability. C₁ should be approximately 100μFD per ampere.



For multiple loads, note recommended connection (Figure Cb). A 1μF decoupling capacitor (C₀) AC-couples the output common to DC ground when a power supply is floated at a DC potential above ground. The DCS series can be floated at a DC voltage of 500VDC maximum.

It is important to note that the high efficiency of the DCS series is maintained over the entire 2:1 input range. The efficiency varies less than 3% over this range. The 100-watt unit, which incorporates the PWM regulation scheme offers a remarkable 75% efficiency even though the derived outputs are *fully regulated*. Consider what this means: the DCS 100-watt, triple-output units only dissipate 35 watts internally vs. 100 watts on comparable units that operate at 50% efficiency! This is a factor of 3:1 over many units presently sold today.



Notes

1. Graph based on normalized efficiency of $\approx 71\%$ at full load.
2. Graph is approximate. Actual performance will depend on the number of outputs, loading distribution, and regulation options.

Figure D

General Specifications (Typical at +25°C, Full Rate)

Range of input voltage for which unit will operate per the specifications.	INPUT VOLTAGE RANGE: 9-18VDC 18-36VDC 36-72 VDC OUTPUT VOLTAGE/CURRENT: (See Page 8)
Maximum deviation of the DC output voltage from its nominal value as set by the factory.	PRESET ACCURACY: ±1% (primary or main channel) ±3% (derived or auxiliary channel)
Adjustment range of primary output using potentiometers in front panel.	EXTERNAL ADJUSTMENT: ±5% Primary Output (Typical)
The ability to sense the output voltage of the supply at the load. This allows compensation for "IR" voltage drops in the power bus.	REMOTE SENSE: 0.5VDC Minimum (See Fig. C)
The percent change in the output voltage as the input voltage varies within its specified limits.	LINE REGULATION: 0.2% over full 2:1 input range
The percent change in the output voltage as the load current varies within its specified limits.	LOAD REGULATION: Primary Output: 0.2% (10% to 100% load) Derived Outputs: .1%-.5% (See Fig. B)
Ratio of the output power to the input power. Usually specified at full load and nominal line voltage.	EFFICIENCY: 71% typical (depends on model) Varies < 3% over 2:1 input range
Minimum load required to keep output within specified limits.	MINIMUM LOAD: 10% on all primary and semi-regulated derived outputs.
	PROTECTION MODES: Input Polarity: Reverse diode shunt with series internal input fuse
A crowbar or other circuit which limits the output voltage when a preset limit is exceeded.	Output Overvoltage: 5V outputs limited to 6.2VDC. All other outputs clamp limited to 130% of rating —recovery automatic.
A monitoring circuit which automatically limits the output current when an overload occurs. There are two common types: a) "Fold Back" — will decrease or fold back the output current to $\cong 50\%$ of rated I_{out} . b) Straight line or constant — will limit the output overcurrent to a constant maximum of 120-160% of rated I_{out} .	Output Overcurrent: Straight line current limit at 120% of rating—recovery automatic. (see Page 8)
The maximum DC voltage which may be applied between input and output without causing damage.	ISOLATION: Input to Output: 1000VDC
Same as above except voltage is applied between primary and derived outputs.	Primary to Derived: 500VDC

otherwise specified)

NOISE:

15mV_{pp} (Bandwidth 5Hz-20kHz) or 0.3% of output, whichever is greater.

50mV_{pp} (5Hz-10mHz) or 1% of output, whichever is greater.
(See Fig. H)

An AC voltage which rides on the DC output voltage measured within the bandwidth specified.

REFLECTED INPUT RIPPLE:

10% of I_{in} max. (RMS)

The peak-to-peak AC current that is "reflected back" to the input lines by switching pulses generated by the converter.

TRANSIENT RESPONSE:

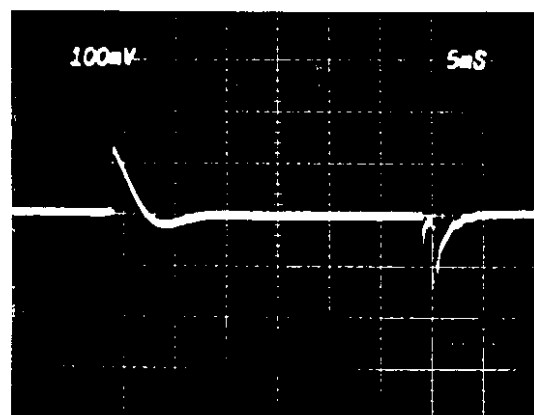
Primary Output:

- 1) Load ≤ 50% to 100% or 100% to 50% maximum deviation ≤ 2.0% nominal V_{out}. Response time ≤ 300μ sec. to 0.5% nominal V_{out}.
- 2) Load 10% to 100% or 100% to 10% maximum deviation ≤ 3%. Response time ≤ 500μ sec. to 0.5% nominal V_{out}.

Derived Output:

- 1) Load ≤ 50% to 100% or 100% to 50% maximum deviation ≤ 10% nominal V_{out}. Response ≤ 800μ sec. to 0.5% nominal V_{out}.
- 2) Load ≤ 10% to 100% or 100% to 10% maximum deviation ≤ 30% nominal V_{out}. Response ≤ 2m sec. to 0.5% nominal V_{out}.

The amount of time required for the output voltage to settle within the regulation limit specified after a step change in output load current.



OSCILLATOR SYNC:

TTL 20mA sink current required.
Sync frequency 18-22kHz.
(See Fig. E)

The ability to synchronize the internal oscillator to an external clock. This is very helpful in telecommunications applications or where the suppression of beat frequencies is essential (See Figure D).

EXTERNAL DISABLE:

TTL high or current source with 20mA capability. Input power at nominal input voltage less than .75W in disable mode. (See Fig. F)

The ability to "shut down" the converter. Very helpful when long periods of inactivity are anticipated (See Figure E).

PARALLEL OPERATION: Yes

(See Fig. G)

SOFTSTART: Yes, occurs when:

- 1) Power is turned on.
- 2) Disable command removed.
- 3) Input returns from OV condition.
- 4) Removal of current limit condition.

Limits the in-rush current during various turn-on modes by varying the duty cycle of a pulse-width-modulator. This is important when other devices are connected to the same input bus.

TEMPERATURE RATINGS:

Operation: -20°C to +80°C.
(Base Plate)

Storage: -40°C to +85°C.

The range of temperature that the unit will operate within specification in a free air environment. Typical temperature rise is 15°C.

TEMPERATURE COEFFICIENT:

Primary Output: 0.01%/°C.

Derived Output: 0.2%/°C

semi-regulated models

0.1%/°C

regulated models

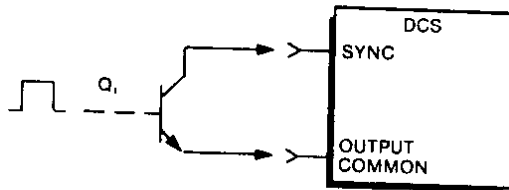
The average change in output voltage as temperature varies from +25°C to the limits specified.

OSCILLATOR SYNCHRONIZATION

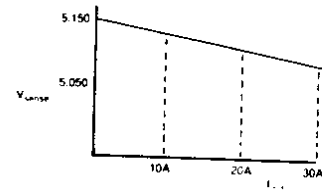
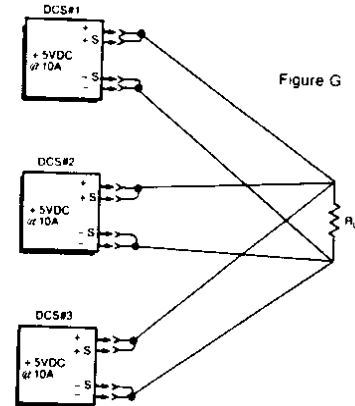
The DCS runs at a switching frequency of approx. 20kHz. To "sync" the DCS from a systems clock, the input to the sync terminal must be a current 'sink' of 10-15mA. Typically, an open collector will suffice. The sync range can be varied $\pm 10\%$ from the nom. Consult factory for higher sync frequency.

- Note: 1. $I = 10\text{-}20\text{mA}$ min.
2. $Q_1 = 2N2222$ or equivalent.

SYNCHRONIZATION
Figure E

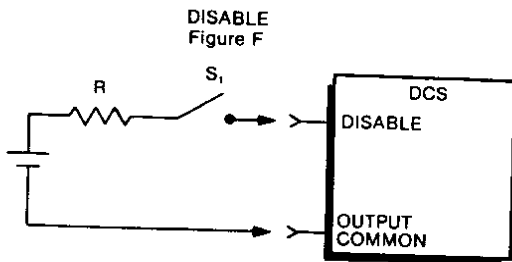


PARALLEL OPERATION (Local Sense - Load Sharing)



EXTERNAL DISABLE

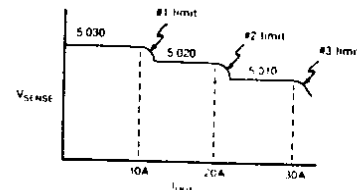
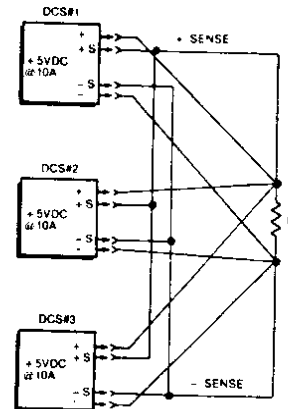
DISABLE
Figure F



The user must provide a 40mA current source with at least 1.5 volts of compliance as shown. If this feature is not to be used, the disable terminal may either be left open or tied to RTN.

- Note: 1. DCS disables when S_1 is closed.

PARALLEL OPERATION (Remote Sense - Load Sharing)



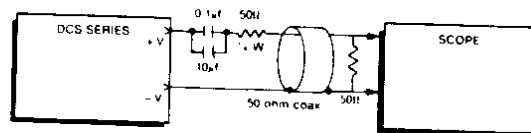
- Note: 1. The example shown is for 3 DCS's rated at 5VDC @ 10 Amps connected in parallel to achieve 5VDC @ 30 Amps at the load.

NOISE MEASUREMENT

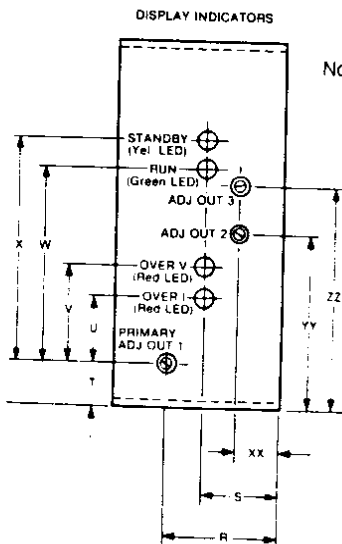
When measuring noise, keep impedance low to minimize pick-up of common-mode switching noise (radiated and conducted at the output). Suggested measurement set-up is shown.

- Note: Ripple = $2 \times$ scope reading.

NOISE AND RIPPLE MEASUREMENT
Figure H



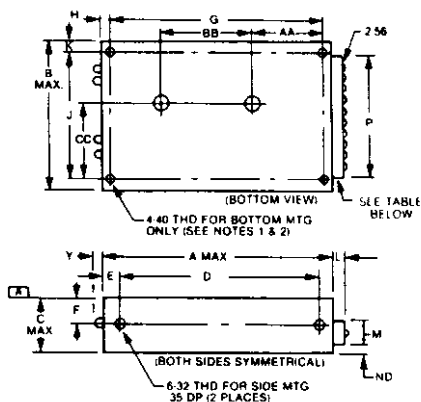
- Note: ADJ Out 2 and 3 on 100 W units only.



DISPLAY FUNCTIONS

CONDITION	INDICATOR STATUS			
	RUN (Green)	STANDBY (Amber)	OVERLOAD (Red)	OVP (Red)
OUTPUT OVP	ON	OFF	OFF	ON
OUTPUT OVERLOAD	ON	OFF	ON	OFF
DISABLE	OFF	ON	OFF	OFF
NORMAL OPERATION	ON	OFF	OFF	OFF

MECHANICAL DIMENSIONS INCHES (mm)



NOTES
 1 ONLY 1 OF 2 SCREWS ON H DIM MAY BE REMOVED FOR A TOTAL OF 3 MTG POSITIONS
 2 MTG HARDWARE NOT SUPPLIED WITH UNIT
 3 NUMBERS DO NOT APPEAR ON TERMINAL BLOCK

DIM	30 WATT	50 WATT	100 WATT	DIM	30 WATT	50 WATT	100 WATT
A	6.55(166.37)	8.05(204.4)	9.00(228.60)	R	1.24(31.49)	1.35(34.29)	1.20(30.48)
B	4.22(107.18)	4.22(107.18)	4.50(114.30)	S	0.82(20.82)	0.93(23.62)	0.80(20.32)
C	1.55(39.37)	2.06(52.32)	2.20(55.88)	T	0.35(8.89)	0.35(8.89)	0.40(10.16)
D	5.60(142.24)	6.10(154.94)	N/A	U	0.80(20.32)	0.80(20.32)	0.80(20.32)
E	0.45(11.43)	1.40(35.56)	N/A	V	1.15(29.21)	1.15(29.21)	1.15(29.21)
F	0.77(19.55)	1.03(26.16)	N/A	W	2.80(71.12)	2.80(71.12)	2.80(71.12)
G	6.00(152.4)	7.40(187.96)	7.50(190.50)	X	3.15(80.01)	3.15(80.01)	3.15(80.01)
H	0.25(6.35)	0.25(6.35)	0.90(22.86)	Y	0.20(5.08)	0.20(5.08)	0.20(5.08)
J	3.70(93.98)	3.70(93.98)	3.70(93.98)	AA	N/A	N/A	2.50(63.50)
K	0.26(6.6)	0.26(6.6)	0.40(10.16)	BB	N/A	N/A	2.50(63.50)
L	0.32(8.1)	0.32(8.1)	0.52(13.21)	CC	N/A	N/A	1.85(46.99)
M	0.64(16.25)	0.64(16.25)	1.12(28.45)	XX	N/A	N/A	0.45(11.43)
N	0.23(5.8)	0.80(20.32)	0.54(13.72)	YY	N/A	N/A	2.05(52.07)
P	3.50(88.9)	3.50(88.9)	4.25(107.95)	ZZ	N/A	N/A	2.60(66.04)

APPROXIMATE WEIGHTS

30 WATT: 1lb. 8oz.

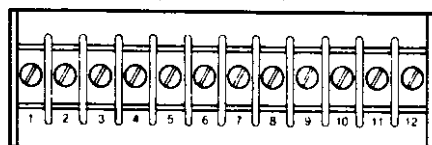
50 WATT: 2lb. 6oz.

100 WATT: 2lb. 8oz.

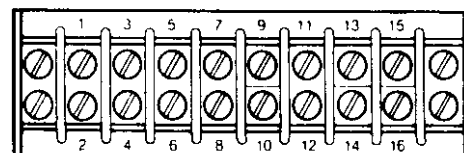
OUTPUT/CONNECTOR DESIGNATION TABLE

MODEL CODES	OUTPUT VOLTAGES	30- and 50-Watt Models			100-Watt Models		
		Output 1	Output 2	Output 3	Output 1	Output 2	Output 3
1	+5	+5			+5		
2	+12	+12			+12		
3	+15	+15			+15		
4	+24	+24			+24		
5	+28	+28			+28		
6	±5	+5		-5	+5		-5
7	±12		+12	-12	+12		-12
8	±15		+15	-15	+15		-15
9	±18		+18	-18	+18		-18
10	+5, +12	+5	+12		+5	+12	
11	+5, +15	+5	+15		+5	+15	
12	+5, +24	+5	+24		+5	+24	
13	+5, +12, -5	+5	+12	-5	+5	+12	-5
14	+5, +15, -5	+5	+15	-5	+5	+15	-5
15	+5, ±12	+5	+12	-12	+5	+12	-12
16	+5, ±15	+5	+15	-15	+5	+15	-15
17	+5, ±18	+5	+18	-18	+5	+18	-18

CONNECTORS
(30 & 50 Watt Models)



100 Watt Models



Terminal	Function 30&50W units	Terminal	Function 30&50W units
1	+ Vin	7	Out 2
2	- Vin	8	Derived Output Return (Out #2 & #3 Common)
3	+ Out 1 Sense	9	Out 3
4	+ Out 1	10	Sync
5	- Out 1	11	Disable
6	- Out 1 Sense	12	Case

Terminal	Function 100W units	Terminal	Function 100W units
1	+ Vin	9	Out 2 Sense
2	+ Vin	10	Out 2
3	- Vin	11	Out 2/3 Com.
4	- Vin	12	Out 2/3 Com.
5	+ Out 1 Sense	13	Out 3 Sense
6	+ Out 1	14	Out 3
7	- Out 1 Sense	15	Sync
8	- Out 1	16	Disable

- Note: 1. Shorting bars provided on terminal blocks are nickel steel. Do not try to pass large currents through these as "IR" drops will occur.
 2. Make sure all terminal screws are tight during operation. Locking washers are recommended.

ORDERING GUIDE

DCS A-XY/Z
 A - Series (30, 50, 100)
 X - Input Code
 Y - Output Code
 Z - Option Code

ORDERING EXAMPLE

DCS 50-2/16
 50 watt DCS
 18-36VDC Input
 + 5VDC, ± 15VDC Outputs

*100W Series available in fully-regulated version only.

OPTION CODES

CODE	OPTION
2	Fully regulated derived output(s), add \$25 (for 1-9 pieces)
4	Extended input range, consult factory
5	Ruggedized version, consult factory

INPUT CODES

CODE	INPUT RANGE
1	9-18VDC (except 100W)
2	18-36VDC
3	36-72VDC

DCS 50-1/15/2

OUTPUT CODE	30-WATT SERIES				PRICE (1-9)	50-WATT SERIES				PRICE (1-9)	100-WATT SERIES				PRICE (1-9)
	OUTPUT VOLTAGE (s)	OUTPUT CURRENT (s) Nom. Min. Max.				OUTPUT VOLTAGE (s)	OUTPUT CURRENT (s) Nom. Min. Max.				OUTPUT VOLTAGE (s)	OUTPUT CURRENT (s) Nom. Min. Max.			
SINGLE OUTPUT															
1	+ 5VDC	6A	0.6A	6A	\$241	+ 5VDC	10A	1A	10A	\$261	+ 5VDC	20A	2A	20A	\$362
2	+ 12VDC	2.5A	0.25A	2.5A	\$230	+ 12VDC	4A	0.4A	4A	\$251	+ 12VDC	8A	0.8A	8A	\$362
3	+ 15VDC	2A	0.2A	2A	\$230	+ 15VDC	3.3A	0.3A	3.3A	\$251	+ 15VDC	6.6A	0.67A	6.6A	\$362
4	+ 24VDC	1.25A	0.12A	1.25A	\$230	+ 24VDC	2A	0.2A	2A	\$251	+ 24VDC	4A	0.4A	4A	\$362
5	+ 28VDC	1A	0.1A	1A	\$230	+ 28VDC	1.8A	0.18A	1.8A	\$251	+ 28VDC	3.6A	0.36A	3.6A	\$362
DUAL OUTPUTS															
6	+ 5VDC - 5VDC	4.8A 1.2A	0.48A 0.12A	4.8A 2.5A	\$267	+ 5VDC - 5VDC	8A 2A	0.8A 0.2A	10A 4A	\$291	+ 5VDC - 5VDC	16A 4A	2A 0.4A	20A 6A	\$419
7	+ 12VDC - 12VDC	1.25A 1.25A	0.125A 0.125A	2.0A 2.0A	\$253	+ 12VDC - 12VDC	2A 2A	0.2A 0.2A	3.2A 3.2A	\$277	+ 12VDC - 12VDC	4A 4A	0.4A 0.4A	5A 5A	\$419
8	+ 15VDC - 15VDC	1A 1A	0.1A 0.1A	1.6A 1.6A	\$253	+ 15VDC - 15VDC	1.7A 1.7A	0.17A 0.17A	2.7A 2.7A	\$277	+ 15VDC - 15VDC	3.4A 3.4A	0.34A 0.34A	5A 5A	\$419
9	+ 18VDC - 18VDC	0.8A 0.8A	0.08A 0.08A	1.38A 1.38A	\$253	+ 18VDC - 18VDC	1.4A 1.4A	0.15A 0.15A	2.3A 2.3A	\$277	+ 18VDC - 18VDC	2.8A 2.8A	0.3A 0.3A	4A 4A	\$419
10	+ 5VDC + 12VDC	3A 1.2A	0.3A 0.12A	4.8A 1.6A	\$267	+ 5VDC + 12VDC	5A 2A	0.5A 0.2A	8A 3A	\$291	+ 5VDC + 12VDC	10A 4A	1.5A 0.4A	16A 5A	\$419
11	+ 5VDC + 15VDC	3A 1A	0.3A 0.10A	4.8A 1.6A	\$267	+ 5VDC + 15VDC	5A 1.7A	0.5A 0.17A	8A 2.8A	\$291	+ 5VDC + 15VDC	10A 3.4A	1.5A 0.34A	16A 5A	\$419
12	+ 5VDC + 24VDC	3A 0.6A	0.3A 0.06A	4.8A 0.8A	\$267	+ 5VDC + 24VDC	5A 1A	0.5A 0.1A	8A 1.6A	\$291	+ 5VDC + 24VDC	10A 2A	1.5A 0.2A	16A 3A	\$419
TRIPLE OUTPUTS															
13	+ 5VDC + 12VDC - 5VDC	3A 0.9A 0.6A	0.3A 0.09A 0.06A	4.8A 1.4A 1.2A	\$289	+ 5VDC + 12VDC - 5VDC	5A 1.5A 1A	0.5A 0.15A 0.1A	8A 2.3A 1.5A	\$331	+ 5VDC + 12VDC - 5VDC	10A 3A 2A	1.5A 0.3A 0.2A	16A 4.6A 3A	\$473
14	+ 5VDC + 15VDC - 5VDC	3A 0.72A 0.6A	0.3A 0.07A 0.06A	4.8A 1.2A 1.2A	\$289	+ 5VDC + 15VDC - 5VDC	5A 1.2A 1A	0.5A 0.12A 0.1A	8A 2A 1.5A	\$331	+ 5VDC + 15VDC - 5VDC	10A 2.4A 2A	1.5A 0.24A 0.2A	16A 4A 3A	\$473
15	+ 5VDC + 12VDC - 12VDC	3A 0.6A 0.6A	0.3A 0.06A 0.06A	4.8A 1.2A 1.2A	\$289	+ 5VDC + 12VDC - 12VDC	5A 1A 1A	0.5A 0.1A 0.1A	8A 1.5A 1.5A	\$331	+ 5VDC + 12VDC - 12VDC	10A 2A 2A	1.5A 0.2A 0.2A	16A 3A 3A	\$473
16	+ 5VDC + 15VDC - 15VDC	3A 0.48A 0.48A	0.3A 0.05A 0.05A	4.8A 0.72A 0.72A	\$289	+ 5VDC + 15VDC - 15VDC	5A 0.8A 0.8A	0.5A 0.08A 0.08A	8A 1.2A 1.2A	\$331	+ 5VDC + 15VDC - 15VDC	10A 1.6A 1.6A	1.5A 0.16A 0.16A	16A 2.4A 2.4A	\$473
17	+ 5VDC + 18VDC - 18VDC	3A 0.42A 0.42A	0.3A 0.04A 0.04A	4.8A 0.6A 0.6A	\$289	+ 5VDC + 18VDC - 18VDC	5A 0.7A 0.7A	0.5A 0.07A 0.07A	8A 1A 1A	\$331	+ 5VDC + 18VDC - 18VDC	10A 1.4A 1.4A	1.5A 0.14A 0.14A	16A 2A 2A	\$473
Total power must not exceed 30 watts.					Total power must not exceed 50 watts.					Total power must not exceed 100 watts.					

NOTE: Until further notice, maximum output current on derived regulated outputs for 30- and 50-Watt Series is 1.5A

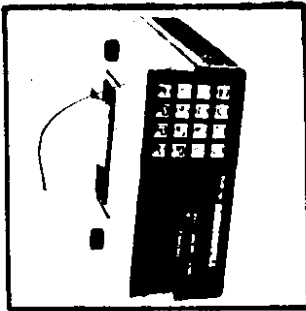
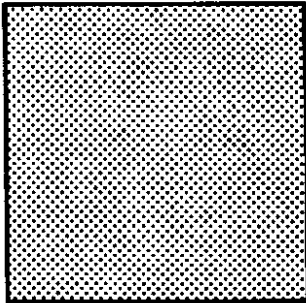
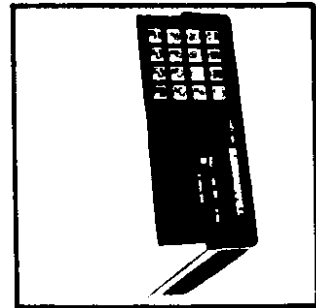
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 1616 BIGELOW AVENUE NORTH
 SEATTLE, WASHINGTON 98109
 (206) 285-2525

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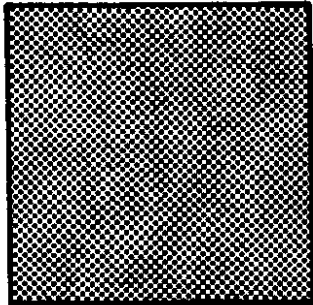
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SAFETY SIGNAL SYSTEMS



NK-1200 SERIES REFERENCE MANUAL

Distance Measuring Equipment

TRAFEGWAY
CEDAR VALLEY, BOX 489 VANDERBILT, PA. 15486-9990 U.S.A.

TRAFEGWAY

Printed in the U.S.A.

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Introduction

Each model in the NK-1200 Series of vehicle installed distance measuring instruments is a powerful microcomputer controlled device with many programmed instructions. Full use of these instruments can be acquired within a short learning and familiarization period. Each model has a built-in TEST MODE feature that simulates sensor signals as though the vehicle is travelling at about 34 m.p.h. While parked, you can use the TEST MODE of operation to become acquainted with the instrument. Depending upon the model, it may take several hours to become totally familiar with the instrument before its full capability can be appreciated. This small investment of time will be repaid 100 fold in more efficient measurements and data collection.

Your instrument was designed by electronic engineers who have had years of experience in actual field measurements of thousands of miles of highway, and actually designed the first electronic distance measurement (DMI) in 1970. Using the first latest "State of the Art" in microprocessor technology, we have been able to incorporate the features and capabilities requested by highway and communication engineers.

To accommodate all the features demanded by many engineers and, at the same time, allow a selection for those requiring only basic distance measuring applications, the NK-1200 Series is available in four (4) models, NK-1201 through NK-1203/P. The operational procedures of each model is described in this manual.

Please keep in mind that each instrument can be up-graded to a higher level without having to purchase a complete new instrument. As an example; if you purchased an NK-1201 and later find a need for the features and capabilities of our NK-1203/P, your 1201 can be up-graded to a 1203/P for the difference in the current list price plus a flat \$50.00 conversion fee.

Section 6 Installation Procedures

Mounting The NK Instrument

Select a suitable location on top of the dashboard and attach the VELCRO strips by removing the self-adhesive protective covering. A matching VELCRO strip is attached to the bottom of the instrument. Each strip should be pressed firmly in place and allowed to set for five minutes prior to mating. Keep in mind that the operator should have a direct line of sight to the display and keyboard. This may require that the instrument be mounted at a slight angle towards the operator.

Plug the cable into the instrument and decide how much slack you will require. There is adequate cable to allow a passenger to hold and operate the instrument if desirable. In the area where the steering column goes through the firewall you can normally find an opening to the engine compartment without having to drill a special hole (speedometer cable, vehicle wiring harness, etc.).

Wiring

1. The location for mounting the terminal block will be under the hood on the left front inner fender.
2. Route all wiring as far as possible from any spark plug wires and ignition coil.
3. Terminate the wiring as shown in Figure M-6. After completion, refer to the OPERATING PROCEDURES SECTION for calibration and operational procedures.

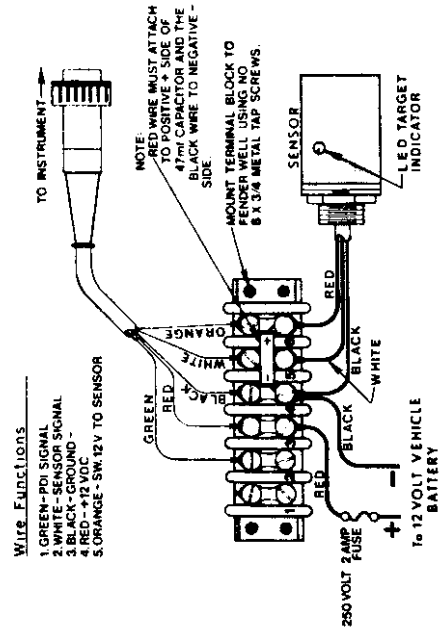


FIGURE M-6

Section 6 Installation Procedures

Wiring For Both Transwawe And Nu-Metrics Instruments

In many instances, it may be desirable to equip a car to accept both the Transwawe NK-1200 Series Instrument and the Nu-Metrics DMI. However, the Transwawe instruments provide the power to the sensor directly from the measuring instrument so when the instrument is OFF (or out of the vehicle) no power is going to the sensor.

With the Nu-Metrics instrument, power to the sensor is supplied by a separate wire connected after the ignition key. In this installation, the sensor is ON anytime the vehicle is being driven.

In order to be able to use both brands in the same vehicle, each instrument wiring harness must be installed as shown in FIGURE M-7. Keep in mind that the orange wire in the NK harness is "HOT" when the NK is turned on. For this reason, you must tape the terminal lug to insure the orange wire does not short to metal or any other wire. Contact of the bare terminal lug will create a direct short which will damage the instrument.

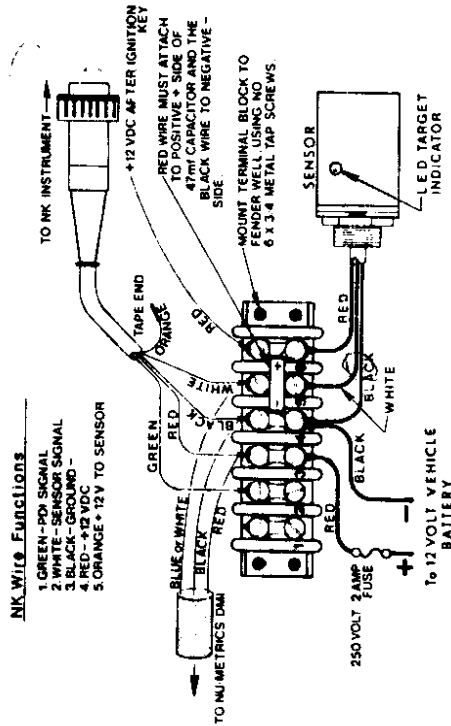


FIGURE M-7

Section 6 Installation Procedures

Transmission Sensor Installation - G.M. Vehicles

1. Remove speedometer cable at the vehicle's transmission. Attach sensor into the transmission using one inch nut. Make sure sensor cable is facing away from the road surface and the exhaust pipe. Insert speedometer cable into back of sensor. Adaptor nut is provided for different thread diameters of the cable.
2. Route the sensor wire to the NK terminal block making sure the wire is not near the exhaust pipe or manifold. Attach leads to terminal block as shown in Figure 1.

NOTE: On G. M. Vehicles equipped with Cruise Control, sensor can be attached to the upper most outlet of the Cruise Control Unit. Terminate wires as described in Step 2.

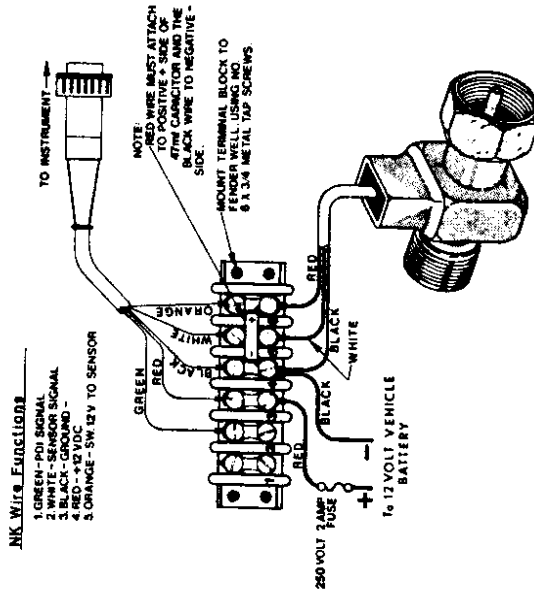


FIGURE 1

If Adaptor Kit is required (Ford and Chrysler vehicles) follow instructions as supplied in the Adaptor Kit, terminate wires as shown in Figure 1.

Switch in front
12 GM 5100
5?

312-792-700

Section 6 Installation Procedures

Wheel Sensor Installation

Mounting Wheel Targets

Ten (10) stainless steel clamp-on targets are provided; however, the maximum you will use is eight (8). The remaining are extras and should be stored in the glove box of the vehicle, should you need them.

STEP 1.

Jack front of vehicle up and remove left front wheel. Lay wheel face down. Targets will be mounted on side of rim that faces under the vehicle.

STEP 2.

Remove all lead wheel weights from this side of rim and move them to the outside, but in the same relative position.

STEP 3.

It is recommended that the rim be thoroughly cleaned with a degreasing solvent or soap and water.

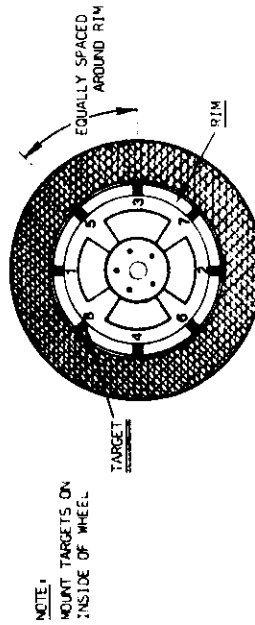


FIGURE M-1

STEP 4.

After the rim is clean, install targets as indicated in Figure M-1. Install the first target on the STEEL CLAMP portion so that the clamp fits between the tire and lip of the wheel rim. The steel clamp holds firmly to the wheel similar to a conventional wheel weight.

NOTE: Caution should be exercised when installing the targets so that the stainless steel portion of the target does not receive a blow (Figure M-2). This could cause the target to separate or could cause non-uniformity in relation to sensor alignment. To install the second target, sight straight across the wheel from the first target and install as described before.

Section 6 Installation Procedures

Halfway between #1 and #2 targets, place #3 target. Sight straight across from #3, place #4 target, etc., until all eight (8) targets are installed. When it becomes necessary to remove the tire from the wheel, the targets should be CAREFULLY removed from the wheel prior to attempting tire removal.

Before re-installing targets on wheel, inspect the spring steel clamp portion of the target. Adjust the clamp with pliers if it appears that it was bent excessively during removal. Squeezing the clamp together will insure a firm, positive fit.

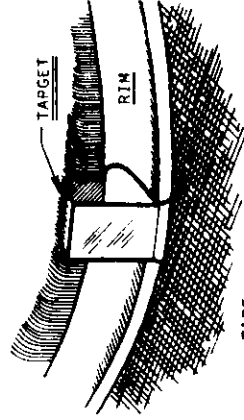
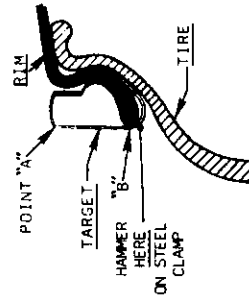


FIGURE M-2

NOTE: The stainless steel portion of the target should be flush with the clip. If there is some separation of the two (B), a light tapping at Point "A" will insure a flush and even target.

Sensor Mounting And Alignment

STEP 1.

Measure the distance from the tie rod end knuckle to the targets. This will give you an idea of how to fashion the bracket for correct scanning of the targets. At this time, you may want to remove the wheel to aid in the installation of the sensor.

STEP 2.

Mount the sensor on the bracket near one end (Figure M-3). The other end will be bolted to the tie rod end using the original nut (a new cotter pin is provided). The distance from the tie rod end to the wheel differs from one vehicle to another. You may have to bend the bracket or cut some off. **NOTE:** On one side of the sensor is a nomenclature plate with an LED light - this side of the sensor should face forward for easy viewing when aligning or checking proper operation. If the wheel has been removed, re-mount the wheel and be sure the face of the sensor is scanning 1/8 inch away from each target.

STEP 3

Route the sensor wire through the fender well to engine compartment. Use cable ties to secure excess cable to the tie rod, making sure there is enough slack in wire so when wheel is turned to extreme left or right it will not break.

STEP 4

IMPORTANT: After the wheel is securely mounted, carefully inspect the proper rotation of the wheel and align sensor accordingly so that each target passes the face of the sensor by approximately 1/8 inch. Also, inspect brake caliper to insure targets have adequate clearance.

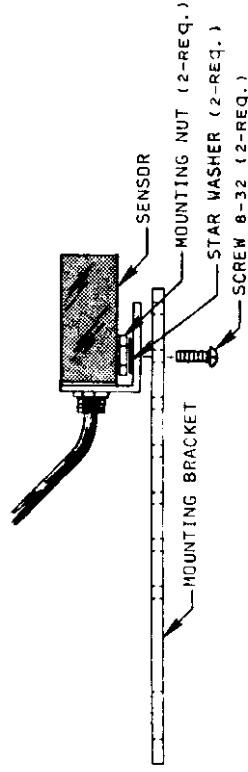
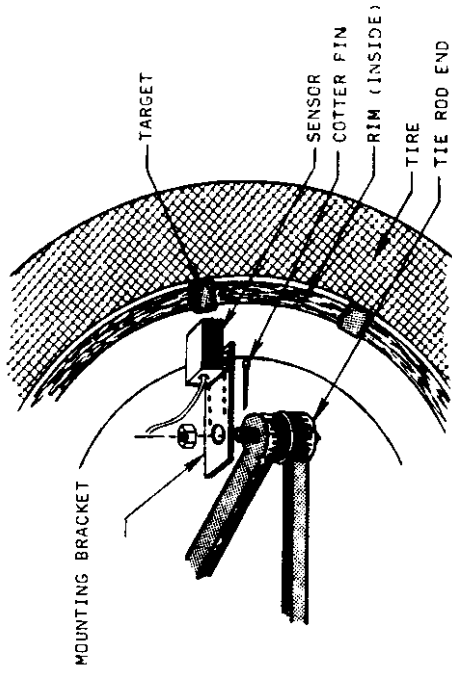


FIGURE M-3

Sensor Installation G.M. Vehicles Equipped With Sway Bar

The typical sensor installation shown in Figure M-3 presents some unique problems when applied to late model General Motors Corporation cars. Although, not readily discernible during installation, the sensor may come into contact with the sway bar when the steering is turned and the suspension is compressed. This causes the sensor to be forced into the targets mounted on the wheel rim. As you may well imagine, when this occurs, two terrible consequences may result. First, the targets may be dislodged or torn completely from the wheel requiring replacement of the affected targets. The second (and most expensive) consequence is that the sensor may be knocked from its mounting bracket, either destroying the sensor and/or the bracket.

To remedy this situation, we have found it necessary to mount the sensor from a position behind the lower ball joint, just below the disk brake caliper. (See Figure M-4). This installation requires a bit more time and mechanical ability than the typical installation. However, the problem-free performance that can be achieved more than compensates for the extra effort expended.

Mechanics Of Installation

STEP 1

The first steps of this installation are, of course, to jack up the left front tire of the vehicle, place a jackstand under the car for safety and remove the wheel. The disk brake pads and caliper must now be removed by taking out the two large allen head bolts and lifting the pads out. The caliper should be supported with a wire and should NOT be allowed to hang by the brake hose.

STEP 2

The next step requires the removal of the disk rotor by first removing the wheel bearing dust cover, cotter key, retaining nut and wheel bearings. This now permits the careful removal of the disk rotor and hub assembly which finally exposes the bolt (5/16-20 x 3/4") that we are searching for. It is located just below the brake caliper on your right and is used to fasten a dust cover to the assembly.

STEP 3

This bolt (5/16-20 x 3/4") should be removed and replaced with a longer bolt (5/16-20 x 1 1/4"), complete with nut and lock washer, so that approximately 1/2" protrudes on the engine side of the assembly. This stud now provides the mounting point for the sensor bracket. After the bolt is secured, the bracket and sensor should be securely mounted using the new nut and lock washer.

STEP 4

39

As illustrated in Figure M-4, the bracket must be bent at a right angle for proper sensor alignment. Some trial and error will be required to properly position the sensor squarely in front of the targets and must be completed after reassembly of the unit.

STEP 5

Careful scrutiny must now be used to insure that no part of the suspension comes into contact with the sensor at both stops of the steering travel. Attention should also be directed to the routing of the cable at this time to insure that it will not become entangled in the suspension or steering.

STEP 6

Reassembly of the unit can now be done by reversing the disassembly sequence. The remainder of the installation can be accomplished as explained in the typical sensor installation.

Typical G.M. Installation

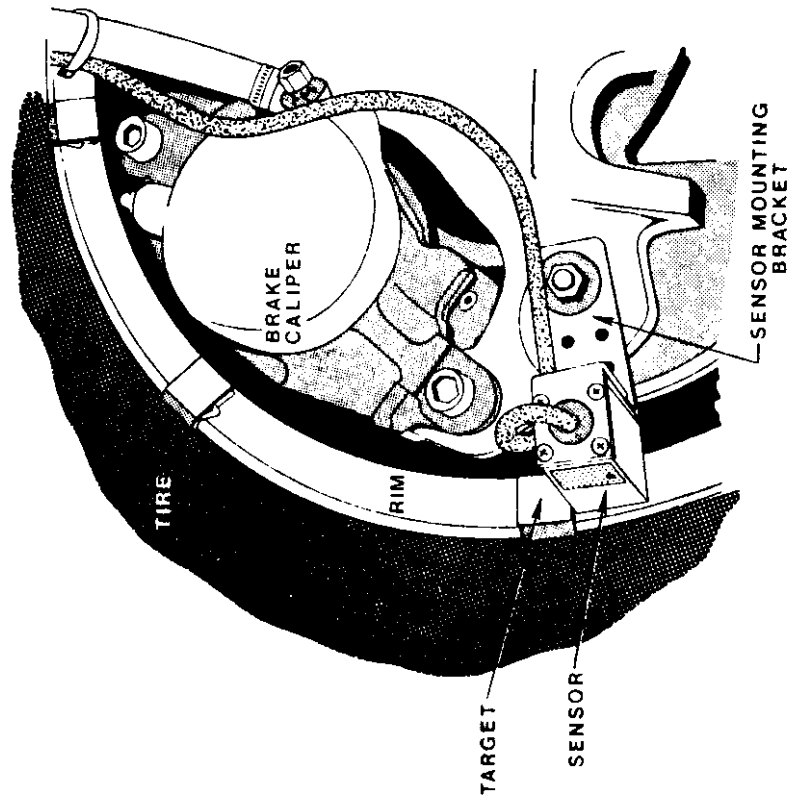


FIGURE M-4

Typical Ford Installation

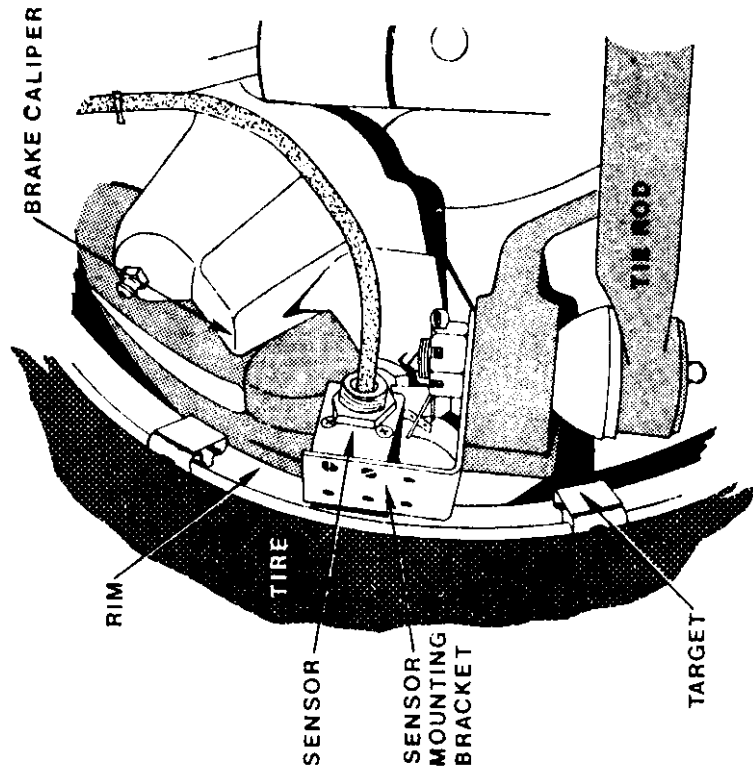


FIGURE M-5

Pre-Calibration Procedures

1. Place the "Power On/Off" switch on the front of the instrument to the "On" position. For a period of about one (1) second, the instrument performs a self diagnostic test during which the instrument will remain blank.
2. When first turned on, the instrument will be in the "STOP" position with the Miles and Meters indicator lights (not functional on the 1201) flashing.

Prior to calibrating the NK to a particular vehicle, tire pressure must be assured. Pressure should be the optimum pressure recommended by the tire manufacturer. For continuous accurate measurements, it is important that the pressure be maintained within ± 2 pounds of the pressure used to calibrate the instrument.

Pre-measure a 1,000 foot long and straight road course accurately with a measuring tape. A shorter course can be used if necessary, i.e.: 600 feet, 800 feet, etc.

Mark the pre-measured course at the beginning and the end with an object. Start and stop with markers at the same sight reference.

Example: At the beginning of course, sight out of the window of the vehicle at the marker, using an object on vehicle as reference, i.e. door handle, window post, radio antenna, etc.

Instrument Calibration—NK-1201

1. Place power switch to "ON". The display should indicate a "0" in the right most digit and the unit will be in the "STOP" mode (Indicator Lights flashing).
2. Depress the "CLEAR" key.
3. Depress the "VSC" key. The number "E5" will be shown on the far left digit.

4. On the keyboard, depress the numbers 1000 in sequence. As you enter each number, it will be displayed and move to the left as each subsequent number is depressed. You are now programming the instrument to count one (1) each time it receives a pulse. In essence, you are merely counting the pulses received from the sensor. The LED's should still be flashing, indicating a "STOP" mode.
5. Depress "ENTER". The value (1000) is now entered into the instrument and the display will drop to zero. The "ES" will be blank.
6. Release the STOP and drive the pre-measured calibration course starting at the beginning and stopping at the end. Depress STOP again to hold the count.

The digital display will read the total number of pulses acquired over the pre-measured course. Mathematically divide this number into 1000 for the actual course length used). The result will be the approximate "VSC" calibration number for measuring distance, i.e. pulse counts of 1035 divided into 1000 equals 966.

Enter the "VSC" number in the sequence of: STOP, CLEAR, VSC, key in VSC value, ENTER. Re-drive the pre-measured course and if the measured distance is too low, use a higher "VSC" number, and, if too high, use a lower "VSC" number.

The value of a previously entered "VSC" number can be viewed while in the STOP mode by depressing the "VSC" key. If the value is to be changed, depress CLEAR, key in the new value, depress ENTER. If the value is not changed, depress ENTER to store the value on display back into the instrument.

Once adjustments have been made and the "VSC" program number is established for the vehicle, it is advisable to write down the program number on a piece of tape and affix it to the vehicle dashboard or sun visor. When power to the NK is turned off, the VSC program number is eliminated from the registers, and must be re-entered in the computer again each time power is restored. This feature serves as a check to insure that the correct VSC number is being used each time the instrument is operated.

Instrument Calibration-NK-1202,NK-1203,NK-1203/P

Unlike the NK-1201 which requires a manual mathematical calculation for determination of the VSC number, the NK-1202, 1203, and 1203/P will automatically determine its VSC calibration number. The procedure for AUTOMATIC CALIBRATION is as follows:

1. Place power switch to "ON". The display should indicate a zero (0) in the right most digit and the instrument will be in the "STOP" mode (LED's flashing).
2. Depress the "CLEAR" key.
3. Release the "START/STOP" key and drive the pre-measured calibration course. During this period, zero (0) will remain on display and no count will be seen.
4. At end of calibration course, depress "STOP" key.
5. Depress "AUTO VSC", followed by length of the calibration course, i.e. 1000, 800, 723, etc.
6. Depress "ENTER". The instrument will calculate and display the appropriate VSC (calibration) number.
7. Depress "ENTER" again. The VSC value is now entered in to the instrument and the length of the calibration course is verified on display.
8. Depress "CLEAR". The instrument is now ready to measure and display actual distance travelled.

If the VSC (calibration) number has already been established, you can enter this number without going through the automatic calibration procedure as follows:

1. Start/stop in STOP mode.
2. Depress "CLEAR" key.
3. Depress "AUTO VSC" key.
4. Depress "CLEAR" again.
5. Key in VSC number.
6. Depress "ENTER".

Re-drive the calibration course to verify that the VSC number is correct, and if the measured distance is too low, use a higher VSC number; if too high, use a lower VSC number.

The value of a previously entered "VSC" number can be reviewed while in the STOP mode by depressing the "AUTO VSC" key. If the value is to be changed, depress CLEAR, key in the new value, depress ENTER. If the value is not changed, depress ENTER to store the value on display back into the instrument.

Once adjustments have been made and the "VSC" program number is established for the vehicle, it is advisable to write down the program number on a piece of tape and affix it to the vehicle dashboard or sun visor. When power to the NK is turned off, the VSC program number is eliminated from the registers, and must be re-entered in the computer again each time power is restored. This feature serves as a check to insure that the correct VSC number is being used each time the instrument is operated.

Section 8 Warranty And Specs.

Limited Warranty

- A. The Transwave NK-1201 through NK-1203/P instruments are covered by a one-year limited warranty on parts and labor against defects in materials and workmanship. Sensors, targets, cables, connectors, brackets and other hardware is warranted for ninety (90) days.
- B. TRANSWAVE CORPORATION warrants each new instrument product manufactured by it to be free from defective material and workmanship and agrees to remedy any such defect or to furnish a new part in exchange for any part of any unit of its manufacture which under normal installation, use and service discloses such defect, provided the unit is returned to our factory or authorized service agent, intact, for examination, with all transportation charges prepaid.
- C. This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, incorrect wiring not our own, improper installation or to use in violation of instructions furnished by us, nor extend to units which have been repaired or altered outside of our factory or authorized service agent.
- D. Any part of a unit approved for remedy or exchange hereunder will be remedied or exchanged by the authorized agent or our factory sales division without charge to the owner.
- E. This warranty is in lieu of all other warranties expressed or implied and no representative or person is authorized to assume for us any other liability in connection with the sales of our products.
- F. TRANSWAVE CORPORATION reserves the right to make improvements in the product specifications at any time without notice.
- G. Questions concerning this warranty or any TRANSWAVE CORPORATION product should be directed to either the Sales or Service Department at (412) 628-6370.

NK-1200

9.01

Section 8 Warranty And Specs.

Specifications-NK-1201

POWER: 9 to 16 VDC, negative ground, 3.6 watt average.
OPERATING TEMPERATURE: 0 degrees C to + 70 degrees C.
DISPLAY: 1.0 ft. to 999,999 ft.
DISTANCE RESOLUTION: \pm 1.0 ft.
ACCURACY: \pm 1 ft. (display) \pm .001 ft. (computation)
KEYBOARD: Touch-Tell 16 Key
PRE-DISTANCE: 0-999,999 feet
SENSOR: Solid State Proximity or Transmission Type
BI-DIRECTIONAL: Compute distance count up or down
DIMENSIONS: 6.1" (W), 6.3" (D), 2.6" (H)
WEIGHT: 14 oz.

Specifications-NK-1202

POWER: 9 to 16 VDC, negative ground, 3.6 watt average
OPERATING TEMPERATURE: 0 degrees C to +70 degrees C.
DISPLAY: 1.0 feet to 999,999 ft.
DISTANCE RESOLUTION: \pm 1.0 ft.
ACCURACY: \pm 1 ft. (display) \pm .001 ft. (computation)
KEYBOARD: Touch-Tell 16 Key
PRE-DISTANCE: 0-999,999 ft., 0-813.440 miles or 0-999,999 kilometers
SENSOR: Solid-State Proximity or Transmission Type
BI-DIRECTIONAL: Compute distance count up or down
UNIT: Automatic Conversion, 0-999,999 ft., 0-999,999 kilometers, 0 - 813.440 miles
VSC (AUTO): Automatic calibration entry
WAYPOINT: Display hold
DIMENSIONS: 6.1" (W), 6.3" (D), 2.6" (H)
WEIGHT: 14 oz.

Section 8 Warranty And Specs.

Specifications-NK-1203

POWER: 9 to 16 VDC, negative ground, 3.6 watt average
OPERATING TEMPERATURE: 0 degrees C to +70 degrees C
DISPLAY: 1.0 ft. to 999,999 ft.
DISTANCE RESOLUTION: \pm 1.0 ft.
ACCURACY: \pm 1 ft. (display) \pm .001 ft. (computation)
KEYBOARD: Touch-Tell 16 Key
PRE-DISTANCE: 0-999,999 ft., 0-813.440 miles or 0-999,999 kilometers
SENSOR: Solid-State Proximity or Transmission Type
BI-DIRECTIONAL: Compute distance count up or down
UNIT: Automatic Conversion, 0-999,999 ft., 0-999,999 kilometers, 0 - 813.440 miles
VSC (AUTO): Automatic calibration entry
WAYPOINT: Display Hold
SPEED: 0-999 MPH, KPH or FPS
MEMORY Two digit code (0 - 99), 10 Memory locations
PRINT-MARK: Direct peripheral control
PDI: TTL positive true user selectable duration .01 sec. to 2.55 sec.
DIMENSIONS: 6.1" (W), 6.3" (D), 2.6" (H)
WEIGHT: 14 oz.

Section 8 Warranty And Specs.

Specifications-NK-1203/P

POWER: 9 to 16 VDC @ 20 watts peak
OPERATING TEMPERATURE: 0 degrees C to +70 degrees C
DISPLAY: 1.0 ft. to 999,999 ft.
DISTANCE RESOLUTION: \pm 1.0 ft.
ACCURACY: \pm 1 ft. (display) \pm .001 ft. (computation)
KEYBOARD: Touch-Tell 16 Key
PRE-DISTANCE: 0-999,999 ft., 0-81.0440 miles or 0-999.999 kilometers
SENSOR: Solid-State Proximity or Transmission Type
BI-DIRECTIONAL: Compute distance count up or down
UNIT: Automatic Conversion, 0-999,999 ft., 0-999.999 meters, 0 - 813.440 miles
VSC (AUTO): Automatic Calibration entry
WAYPOINT: Display hold
SPEED: 0-999 MPH, KPH or FPS
MEMORY: Two digit code (0 - 99), 10 Memory locations
PRINT-MARK: Direct peripheral control
PDI: TTL positive true user selectable duration .01 sec. to 2.55 sec.
PRINTER: Alpha Numeric Dot Matrix 5 x 7, 16 column
PRINT SPEED: 1 Line/Sec.
PAPER: Standard 1.8" W
RIBBON: Inked Cassette
DIMENSIONS: 6.1" (W), 6.3" (H), 2.6" (D)
WEIGHT: 1.2 lbs.

INTRODUCTION

The HT/1000 is an extremely versatile handheld terminal. Much of this flexibility is due to the programmable communications, keyboard, and display options designed into the unit.

With all the features available to the user it is recommended that this manual be thoroughly reviewed prior to integrating the HT/1000 into the user's system.

This manual has been written with a detailed explanation of each operation. Its intent is to quickly and easily familiarize the user with the terminal. In addition, information has been included on the available communications interfaces and on battery life characteristics. We feel that this should facilitate easy integration of the HT/1000 into your system. However, should you require further assistance on any matter, please contact the factory and we will provide you with any support necessary.

HT/1000 VERSIONS

HT/1000 OEM -

Because there are times when the great flexibility of the HT/1000 is not needed, Termiflex has another model, the HT/1000 OEM. This is a simplified version of the HT/1000 available in quantities of 40 and above. The keyboard, display, and interfaces remain the same as the standard model, but the HT/1000 OEM will not have operating batteries, a backup battery, a wide range power supply or user selectable options. The advantage of the HT/1000 OEM is its lower per unit pricing. It is also available with the user customizable keyboard if you wish to make your own nomenclature.

HT/1000K -

The HT/1000K is identical in operation to the HT/1000. This version provides the user with the means to customize the keyboard to suit the projects needs.

When the user receives the terminal, there will be three additional pieces in the carton. One is the write-on layer which the user will apply custom lettering to. The other piece provides the tactile feedback for the membrane switch and protect the custom lettering. The third piece is a transfer lettering kit which can be used to customize the write-on layer. This kit or any other suitable means may be used.

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WARRANTY

Products manufactured by TERMIFLEX CORPORATION are warranted to the original purchaser against defective materials and workmanship for a period of one year from purchase - under normal use and service. This warranty is void where a product has been damaged by accident or abuse, or if the serial number is altered or removed, or if the product has been serviced, or modified by other than an authorized representative of TERMIFLEX CORPORATION.

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WARNING:

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to correct the interference.



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18 Airport Road
Nashua, New Hampshire 03063 USA
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TWX: 710-228-7545

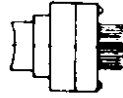
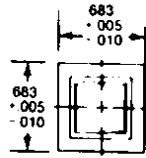
Terminflex

HT/1000

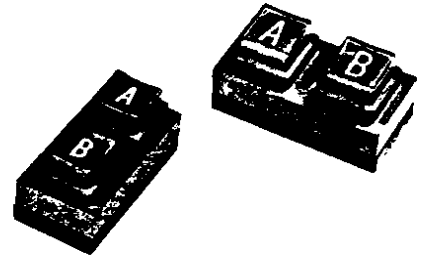
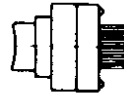
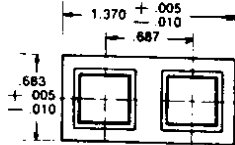
USER'S MANUAL

Series 82 Standard Keyboard Modules

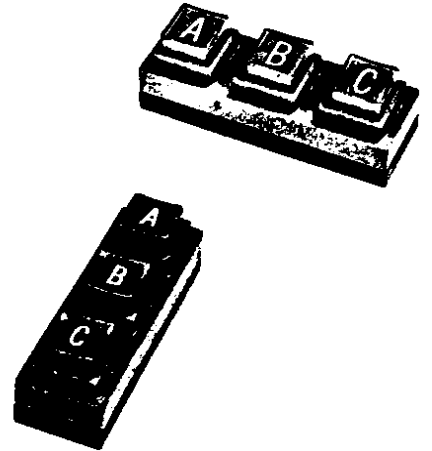
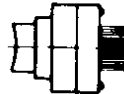
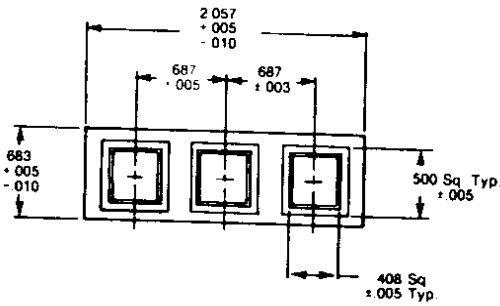
One Button Module



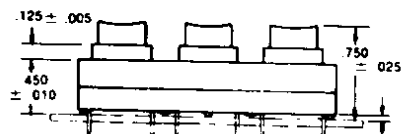
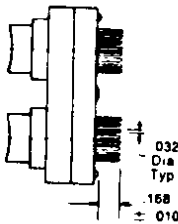
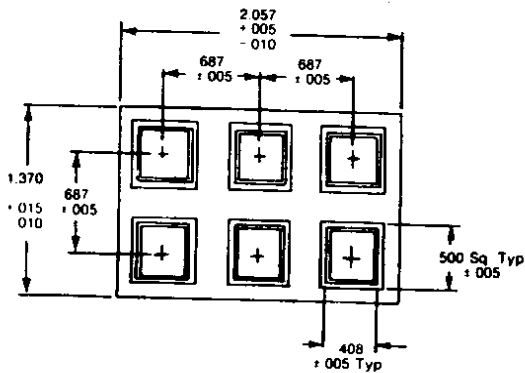
Two Button Module



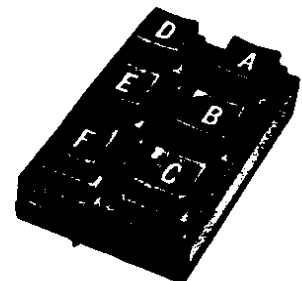
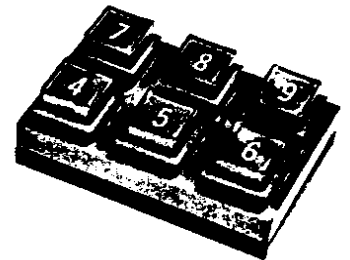
Three Button Module



Six Button Module



Circuit Board Standoff
 $.062 \pm .005 \text{ Dia} \times .032 \pm .005 \text{ High}$

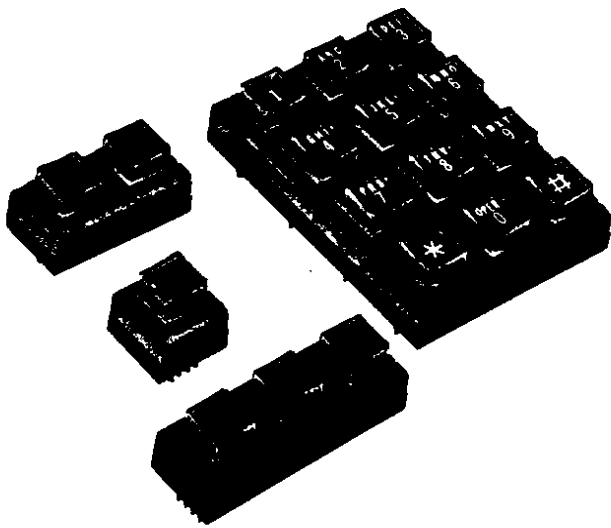


For rear views, see page 22.

Patent No.
 3, 818, 169.

Stack In Any Array

- 11/16 Inch Button Centers Maintained With Modules Placed Side By Side
 - Vertical or Horizontal Mount
 - Long Stroke, Wiping Contact
 - PC Mountable



Standard Modules

- 1 to 4 Poles Per Button
- Off the Shelf Availability
- Coding Capability
- Choice of Colors and Legend Styles

Lightable Modules

- 1 or 2 Poles Per Button
- Self Legendable
- Mounts Over LED or Lamp

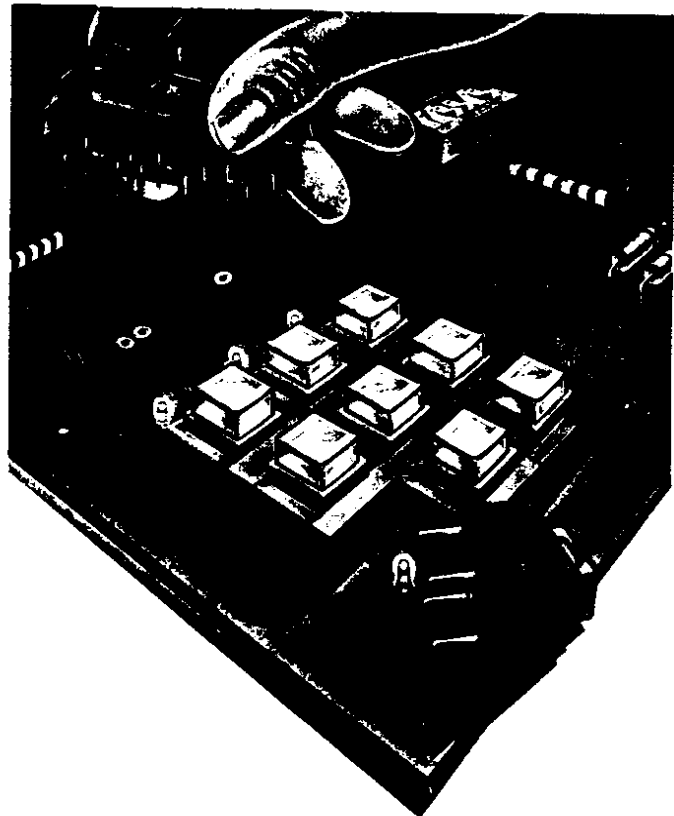


FIGURE 9 – SINGLE PULSE OUTPUT CIRCUIT

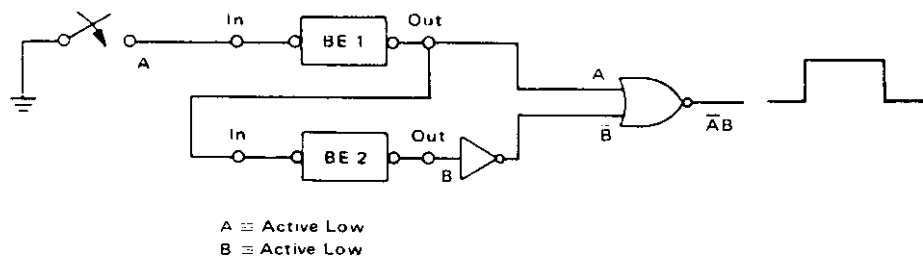
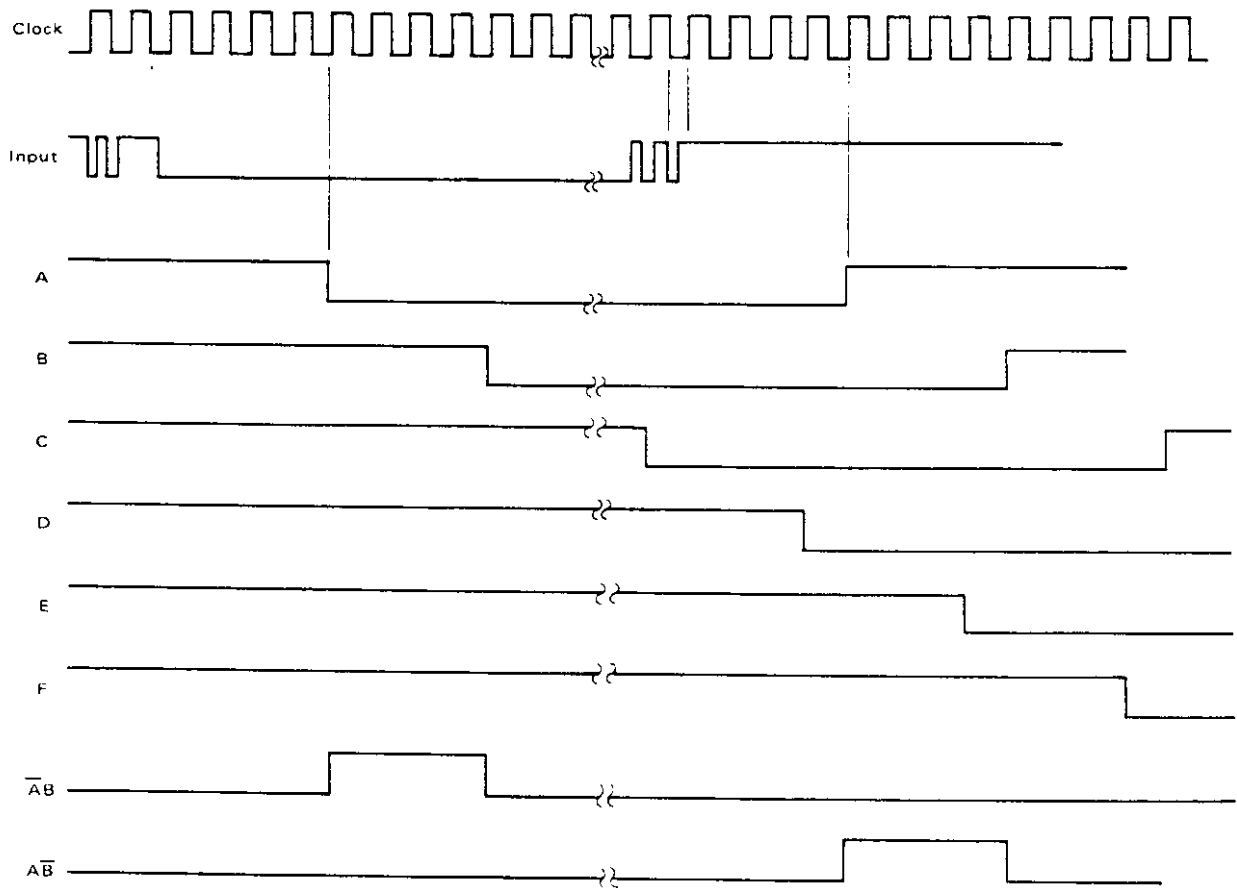


FIGURE 10 – MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM

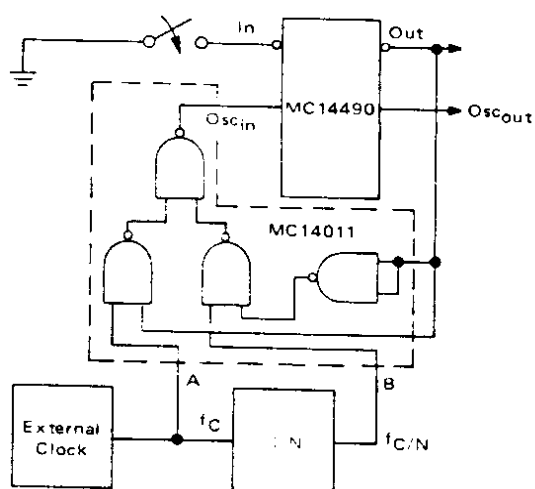


TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

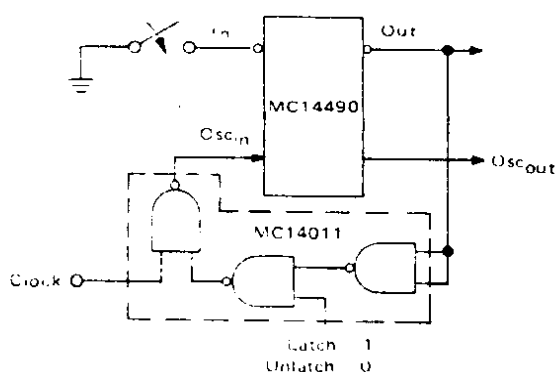
FIGURE 6 - FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 - LATCHED OUTPUT CIRCUIT



MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal \overline{AB} as shown in Figures 9 and 10. The signal \overline{AB} is four clock periods in length. If the inverter is switched to the A output, the pulse \overline{AB} will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 - MULTIPLE TIMING CIRCUIT CONNECTIONS

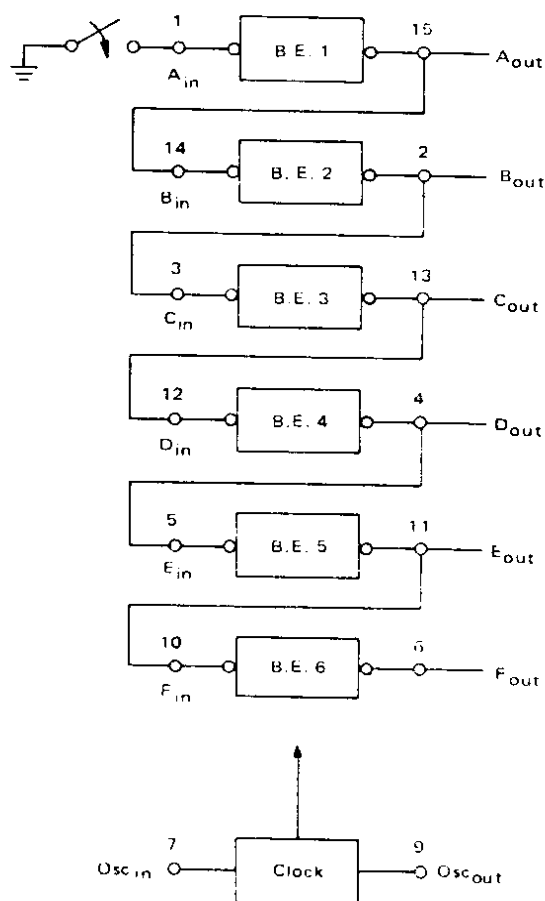
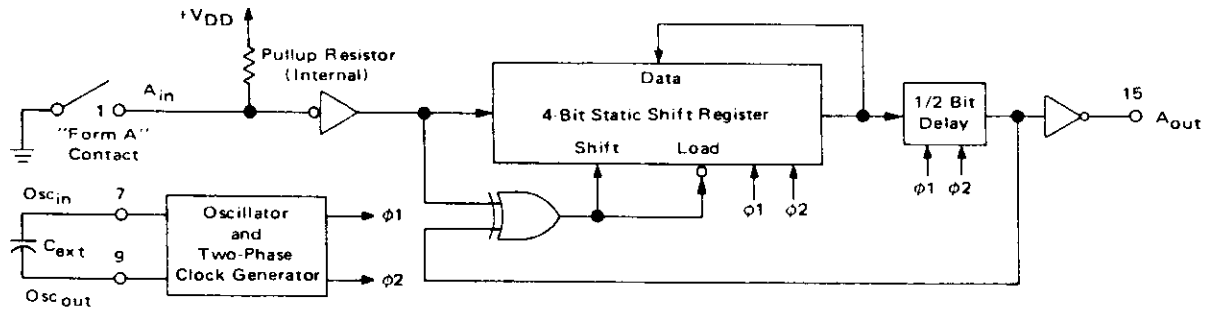


FIGURE 4 – TYPICAL "FORM A" CONTACT DEBOUNCE CIRCUIT
(Only One Debouncer Shown)



OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

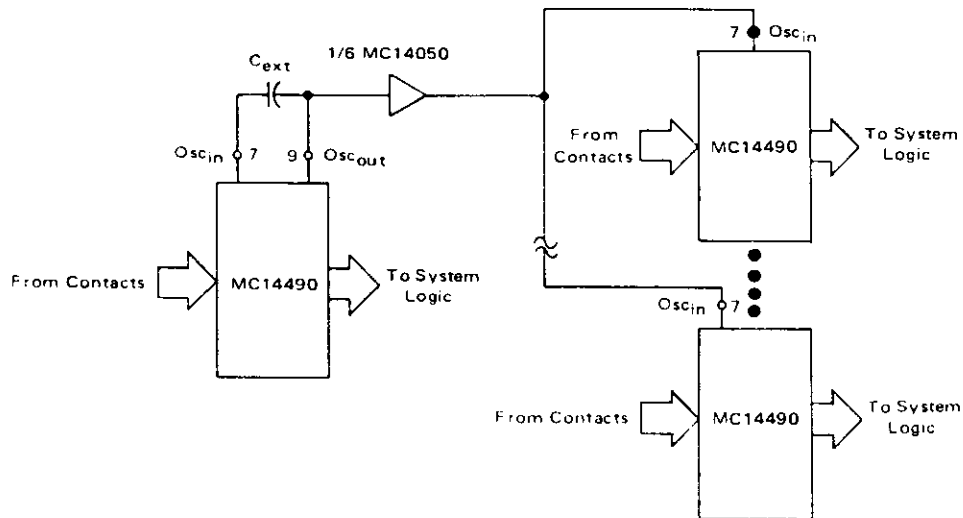
Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with

paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

FIGURE 5 – TYPICAL SINGLE OSCILLATOR DEBOUNCE SYSTEM



THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a $4\frac{1}{2}$ -bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open the shift register is loaded with a 1 (positive logic assumed) on each positive edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with 1's and the output is at a 1 or high level.

At clock edge 1 (Figure 3) the input has gone low and a 0 (low level) has been loaded into the first bit or storage location of the shift register. Just after the positive edge of clock 1 the input signal has bounced back to a logic 1. This causes the shift register to be reset to all 1's in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus a logic 0 has been shifted into all four shift register bits and, as shown, the output goes to a 0 during the positive edge of clock pulse 6.

It should be noted that there is a $3\frac{1}{2}$ to $4\frac{1}{2}$ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N+7 a 1 is loaded into the first bit. Just after N+7, when the input bounces low, all bits are reset to 0. At N+8 nothing happens because the input and output are low and all bits of the shift register are 0. At time N+9 and thereafter the input signal is a high (1) clean signal. At N+13 the output goes high (1) as a result of four 1's being shifted into the shift register.

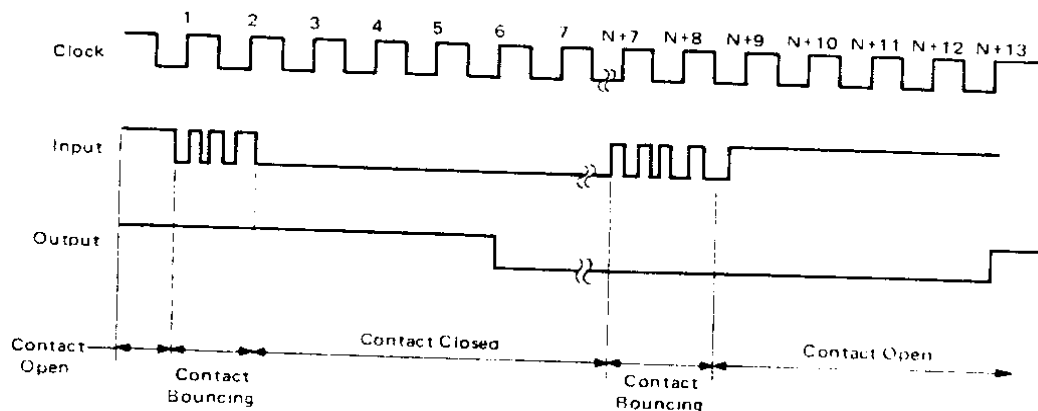
Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if you include the leading edge bounce in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

FIGURE 3 — TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	VDD Vdc	Min	Typ	Max	Unit
Output Rise Time All Outputs	t _{TLH}	5.0	-	180	360	ns
		10	-	90	180	
		15	-	65	130	
Output Fall Time Oscillator Output	t _{FHL}	5.0	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
	Debounce Outputs	5.0	-	60	120	
		10	-	30	60	
		15	-	20	40	
Propagation Delay Time Oscillator Input to Debounce Outputs	t _{PHL}	5.0	-	285	570	ns
		10	-	120	240	
		15	-	95	190	
	t _{PLH}	5.0	-	370	740	
		10	-	160	320	
		15	-	120	240	
Clock Frequency (50% Duty Cycle) (External Clock)	f _{cl}	5.0	-	2.8	1.4	MHz
		10	-	6	3.0	
		15	-	9	4.5	
Setup Time (See Figure 1)	t _{su}	5.0	100	50	-	ns
		10	80	40	-	
		15	60	30	-	
Maximum External Clock Input Rise and Fall Time Oscillator Input	t _{r, tf}	5.0	No Limit		ns	
		10				
		15				
Oscillator Frequency OSC _{out} C _{ext} = 500 pF to 0.1 μF	f _{osc, typ}	5.0	1.5		Hz	
			C _{ext} (in μF)			
			4.5			
			C _{ext} (in μF)			
		15	6.5			
			C _{ext} (in μF)			

FIGURE 1 - TYPICAL SWITCHING TIME WAVEFORMS

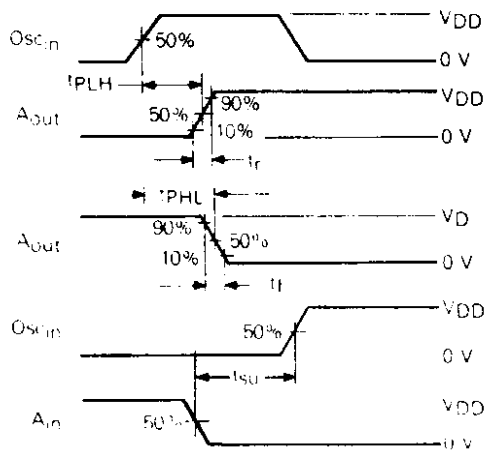
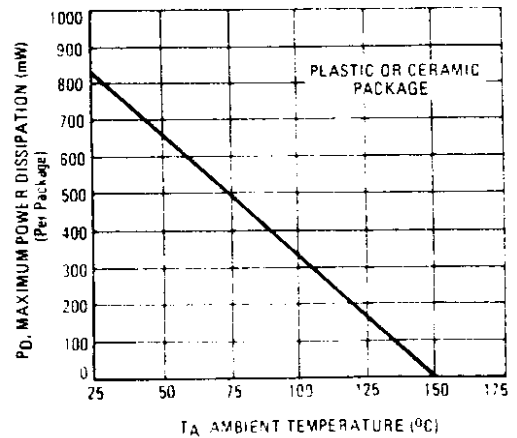


FIGURE 2 - AMBIENT TEMPERATURE POWER DERATING



MAXIMUM RATINGS (Voltages referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	V
Input Voltage, All Inputs	V_{in}	-0.5 to $V_{DD} + 0.5$	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	-55 to +125	$^{\circ}C$
Storage Temperature Range	T_{stg}	-40 to +85	$^{\circ}C$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

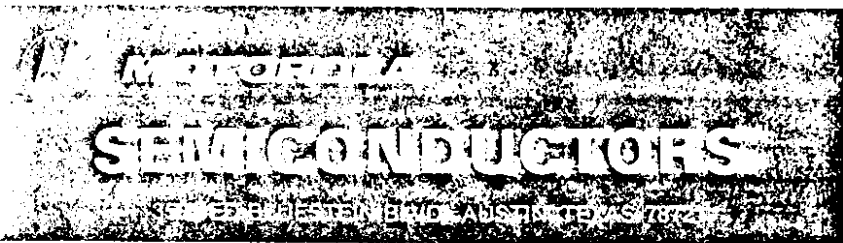
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}^*		25 $^{\circ}C$			T_{high}^*		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0	V_{OL}	5.0		0.05	-	0	0.05	-	0.05	V
		10		0.05	-	0	0.05	-	0.05	
$V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	V
		10	9.95	-	9.95	10	-	9.95	-	
Input Voltage # ($V_O = 4.5$ or 0.5 V) ($V_O = 9.0$ or 1.0 V) ($V_O = 13.5$ or 1.5 V)	V_{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	V
		10	-	3.0	-	4.50	3.0	-	3.0	
(V _O = 0.5 or 4.5 V) (V _O = 1.0 or 9.0 V) (V _O = 1.5 or 13.5 V)	V_{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	V
		10	7.0	-	7.0	5.50	-	7.0	-	
Output Drive Current Source Oscillator Output ($V_{OH} = 2.5$ V) ($V_{OH} = 4.6$ V) ($V_{OH} = 9.5$ V) ($V_{OH} = 13.5$ V) Debounce Outputs ($V_{OH} = 2.5$ V) ($V_{OH} = 4.6$ V) ($V_{OH} = 9.5$ V) ($V_{OH} = 13.5$ V)	I_{OH}	5.0	-0.6	-	0.5	1.5	-	-0.4	-	mA
		5.0	-0.12	-	0.1	0.3	-	-0.08	-	
Sink Oscillator Output ($V_{OL} = 0.4$ V) ($V_{OL} = 0.5$ V) ($V_{OL} = 1.5$ V) Debounce Outputs ($V_{OL} = 0.4$ V) ($V_{OL} = 0.5$ V) ($V_{OL} = 1.5$ V)	I_{OL}	5.0	0.36	-	0.30	0.9	-	0.24	-	mA
		10	0.9	-	0.75	2.3	-	0.6	-	
Input Current Debounce Inputs ($V_{in} = V_{DD}$)	I_{IH}	15	-	2	-	0.2	2	-	11	μA
Input Current Oscillator	I_{in}	15	-	+620	-	+255	+400	-	+250	μA
Startup Resistor Source Current Debounce Inputs ($V_{IL} = V_{SS}$)	I_{II}	5.0	270	375	140	190	255	70	130	μA
		10	415	540	280	380	500	145	265	μA
		15	610	790	415	570	750	215	400	μA
Input Capacitance ($V_{in} = 0$)	C_{in}					5.0	7.5			pF
Quiescent Current	I_{DD}	5.0		150		40	100		90	μA
		10		250		90	225		180	μA
		15		400		225	680		450	μA

*Note: All values specified for worst case combination.
 †Noise margin for both L and H levels: 1.0 V min @ $V_{DD} = 5.0$ V
 2.0 V min @ $V_{DD} = 10$ V
 2.5 V min @ $V_{DD} = 15$ V

* $T_{low} = -55^{\circ}C$ for L Device, $-40^{\circ}C$ for P Device
 $T_{high} = +125^{\circ}C$ for L Device, $+85^{\circ}C$ for P Device





MC14490

HEX CONTACT BOUNCE ELIMINATOR

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V

CMOS LSI (LOW-POWER COMPLEMENTARY MOS)

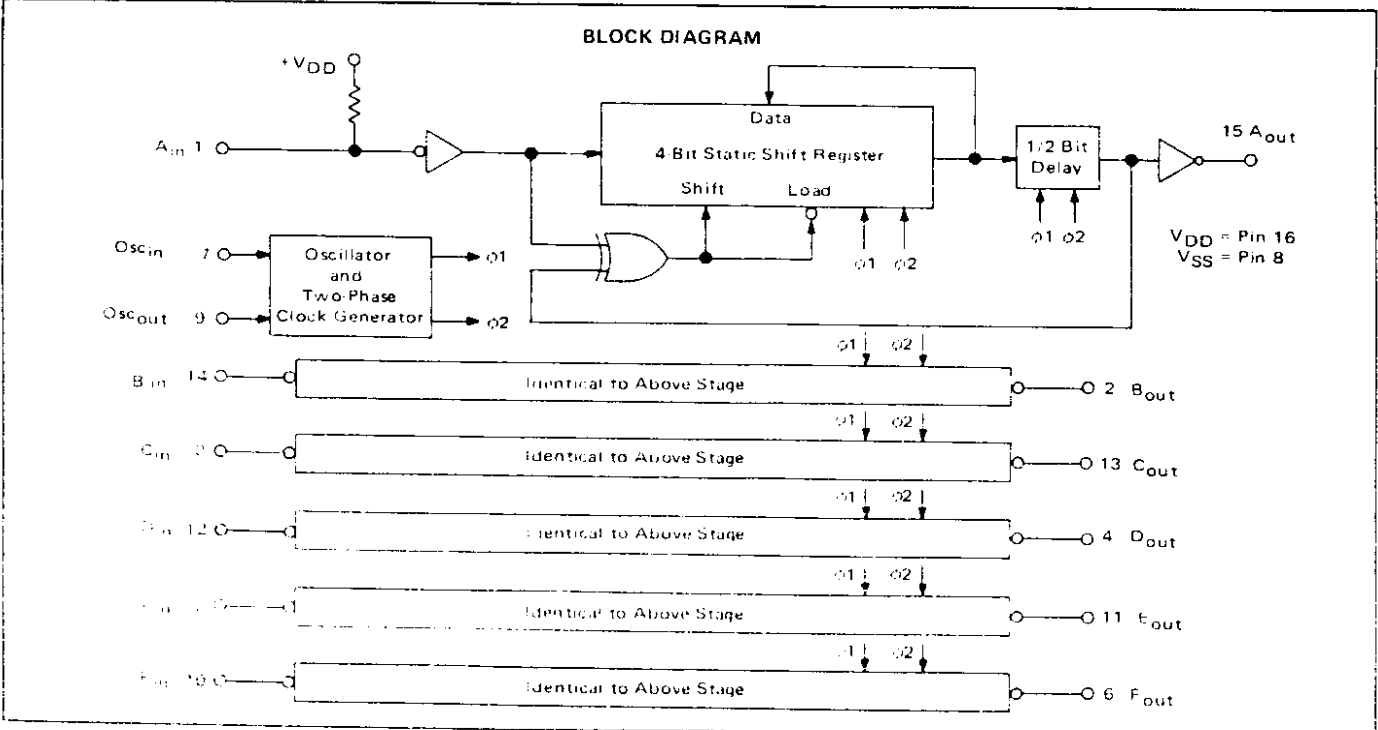
HEX CONTACT BOUNCE ELIMINATOR

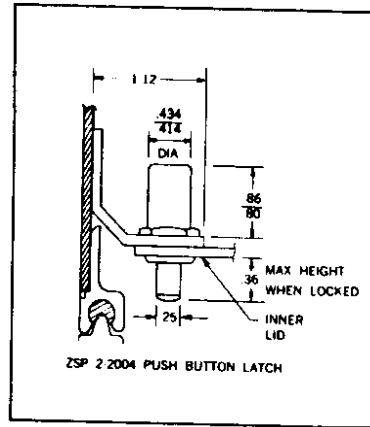
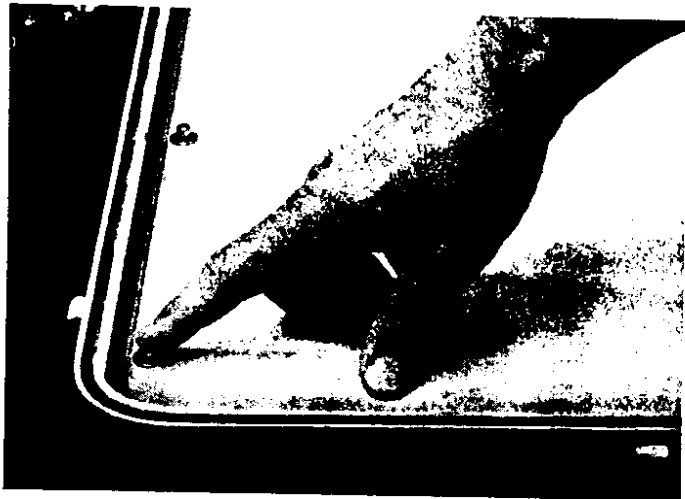
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

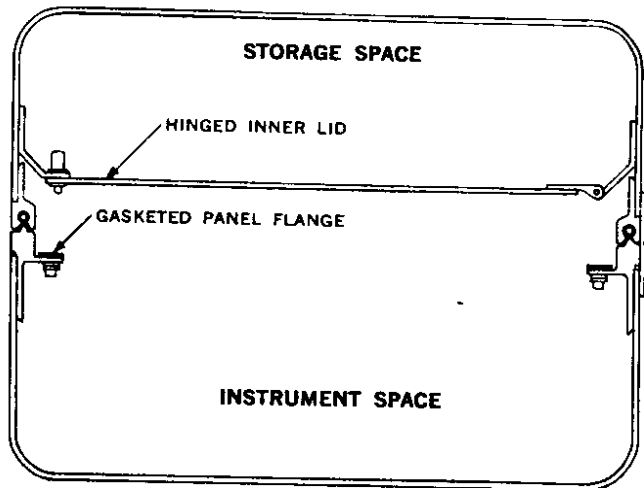
MC14xxx	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package





To determine approximate weight of Inner Lid Assembly, multiply the square foot area by .889 lbs. per square foot for .063 cases; 1.27 lbs. per square foot for .090 cases.

Hinged aluminum inner lids are available in all Zero VAL-AN cases to make the upper part of the case into a storage compartment. The inner lid is secured with a special push button latch that has been tested to 200 pounds.

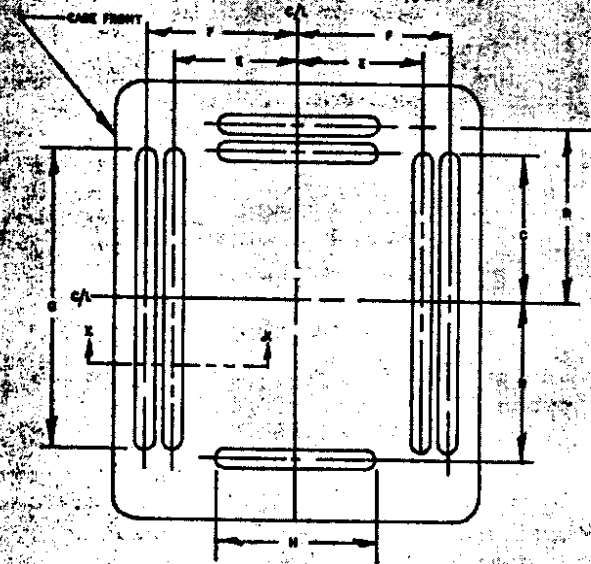


BEADING PATTERNS

beaded as indicated for strength.

Bead pattern in drawing shows top of container. For bottom of case, reverse short beads.

CASE NUMBER	B	C	D	E	F	G	H
BZ	12.19	11.56	12.94	4.00	5.50	22.88	5.25
CC	7.00	6.25	7.75	4.25	6.00	12.75	6.75
CF	8.31	7.56	9.06	5.75	7.25	15.13	9.50
CJ	7.75	7.00	8.50	5.78	7.25	14.00	8.00
KR	10.06	9.31	10.81	4.31	5.81	18.88	6.13
LA	12.88	12.19	13.56	4.59	6.22	26.88	6.94
LK	10.50	9.75	11.25	5.25	6.75	19.75	7.50
LN	9.25	8.50	10.00	5.38	7.00	18.50	8.00
LS	8.00	7.25	8.75	6.56	8.06	14.50	11.13
LV	12.94	12.06	13.56	6.06	7.56	24.38	9.88
LY	7.50	6.75	8.00	5.88	7.13	13.75	8.75
MB	12.38	11.63	13.00	6.88	8.13	24.75	9.00
ME	8.00	7.50	8.75	7.50	8.75	16.00	9.50



Section B-B

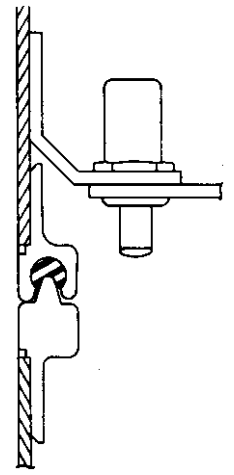
CLOSURE, PANEL FLANGE AND INNER LID DETAILS

Special mating gasketed extrusions are used to provide effective sealing of Zero VAL-AN cases. In addition to sealing, these exclusive closures provide effective alignment of the two halves of the case and protection of the seal and hinges from shearing forces. Each of the closure, panel flange and inner lid choices listed below is available on every VAL-AN case. Specify by inserting the indicated code in the basic part number.

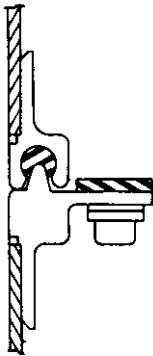
Note: For detailed dimensioning of closure extrusions see pages 168-171.



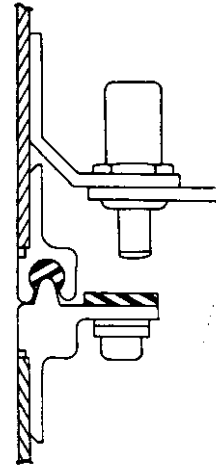
A= Plain.
Weight: .063 cases = .280 lbs/ft.;
 .090 cases = .492 lbs/ft.



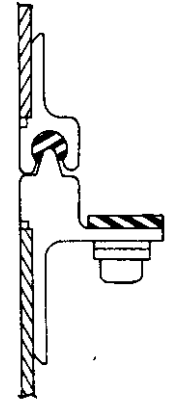
B= Plain with inner lid.
Weight (closure only):
 .063 cases = .280 lbs/ft.;
 .090 cases = .492 lbs/ft.



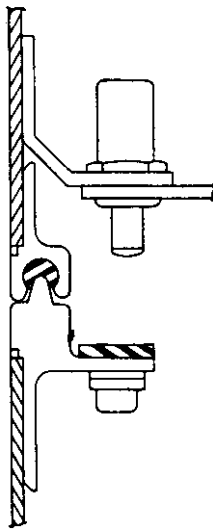
C= Top flanged with nut plates and flange gasket.
Weight: .063 cases = .487 lbs/ft.;
 .090 cases = .737 lbs/ft.



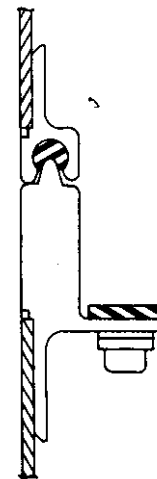
D= Top Flanged with nut plates, flange gasket and inner lid.
Weight (closure and panel flange only): .063 cases = .487 lbs/ft.; .090 cases = .737 lbs/ft.



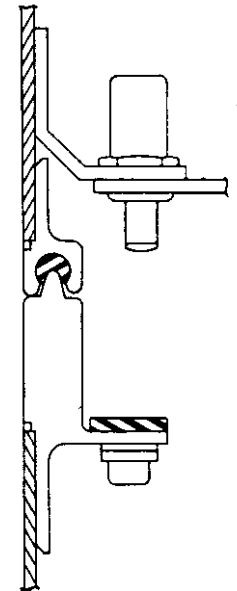
E= Medium recessed flange with nut plates and flange gasket.
Weight: .063 cases = .523 lbs/ft.;
 .090 cases = .744 lbs/ft.



F= Medium recessed flange with nut plates, flange gasket and inner lid.
Weight (closure and panel flange only): .063 cases = .523 lbs/ft.; .090 cases = .744



G= Deep recessed flange with nut plates and flange gasket.
Weight: .063 cases = .887 lbs/ft.;



H= Deep recessed flange with nut plates, flange gasket and inner lid.
Weight (closure and panel flange only): .063 cases = .887 lbs/ft.; .090 cases = 1.122

VAL-AN CASES

SEAMLESS DEEP DRAWN ALUMINUM CONSTRUCTION. 52 LENGTH AND WIDTH COMBINATIONS—THOUSANDS OF DEPTHS TO CHOOSE FROM. SEE PAGES 189-214.

CONTINUOUS MATING GASKETED EXTRUDED CLOSURE. SEE PAGE 216.

H₁ IN 1/4" INCREMENTS

H₂ IN 1/4" INCREMENTS

HANDLES MEET OR EXCEED MILITARY SPECIFICATION ARE LOCATED FOR EASE OF CARRYING. SEE PAGE 215.

MILITARY SPECIFICATION SEE PAGE 219.

SOLID FEET. See Page 218.

HINGED LATCH INNER LID ASSEMBLY. SEE PAGES 216-217.

OPTIONAL PANEL FLANGE (WITH PLATE NUTS, NEOPRENE GASKET AND FREE PANEL TEMPLATE). SEE PAGE 216.

CHOICE OF MANUAL OR AUTOMATIC PRESSURE RELIEF VALVE, SEE PAGE 218.

SPRING LOADED LATCHES TESTED TO 400 POUNDS PULL, ARE LOCATED TO INSURE CASE INTEGRITY. SEE PAGE 215.

NOTE: LENGTH, WIDTH AND HEIGHT ARE OUT-SIDE DIMENSIONS MEASURED AT POINTS OF TANGENCY OF BOTTOM, TOP AND SIDES.

MEETS MIL-STD-108

Zero VAL-AN cases are the result of an intensive design and testing program and will meet or exceed all watertight requirements of MIL-STD-108.

ZERO-WEST: U.S. GOVERNMENT PROCUREMENT VENDOR CODE NUMBER 98376
ZERO-EAST: U.S. GOVERNMENT PROCUREMENT VENDOR CODE NUMBER 19178

CODE CASE TYPE

- 1 = Combination Case (No feet on rear except when handle is on front. Latches on case with strikes on cover. Separable hinges).
- 2 = Transit Case (No feet on rear except when handle is on front. Latches are on cover, strikes on case. Non-separable hinges).
- 3 = Instrument Case (Feet on rear and bottom in all situations. Separable hinges).

Note: Drawings shown on pages 189-214 are typical subject to the above.

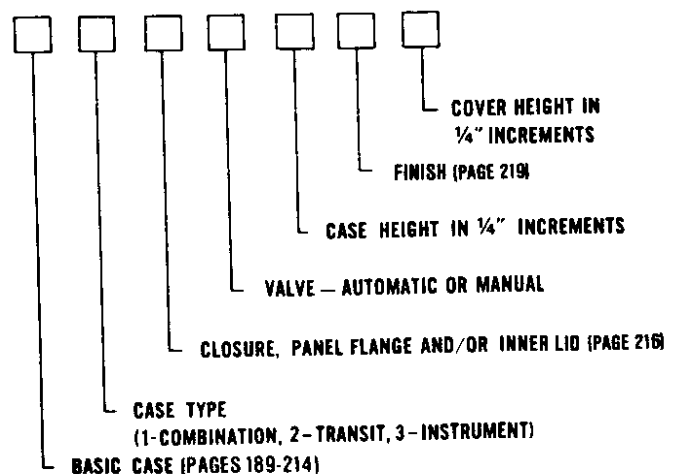
HOW TO USE THIS CATALOG SECTION.

This catalog has been designed to speed and simplify ordering watertight cases to MIL-STD-108. Choose the basic case size, specify combination, transit or instrument case, indicate manual or automatic pressure relief valve, case and lid height and finish desired by inserting the code for each in the basic part number formula below. Cases are supplied without panel. Panels may be ordered separately.

Part Number Example

HG1DA20C18

specifies a deep drawn aluminum combination case, 9" x 27", to comply with MIL-STD-108, with one handle, four latches, two hinges, gasketed closure with flush panel flange complete with 10-32 floating nut plates and neoprene gasket, hinged and latched inner lid, automatic two-way pressure relief valve, case 5" high, cover 4 1/2" high, painted per MIL-E-15090, Type III, Class 2, light gray semi-gloss enamel.



UNPACKING & STARTUP

1.1 UNPACKING

Your HT/1000 is ready to operate from the moment you unpack it. Nothing needs to be done to it except plug it into an appropriate mating connector. However, we recommend that you examine the package carefully to be certain everything is there. Included in the box there should be:

- a) One HT/1000 Control/Display Unit
- b) One HT/1000 User's Manual
- c) Six size AA alkaline batteries

OPTIONS

- a) One optional cable
- b) Six rechargeable nickel cadmium AA batteries
- c) One rechargeable battery charger

Install the batteries being careful to observe the polarities. If either the rechargeable battery option or an optional cable were ordered, please refer to the option installation instructions.

When the unit is powered up, the display will go through a self-test of displaying a full screen of each "#", "M", "I", and sounding the buzzer. Then the cursor will either be a solid black block indicating that the unit is waiting for a "CTS" signal (If RS-232-C) or it will be a small open block indicating that the unit is ready to operate. See "Display Operation" for further cursor information.

The default

parameters are: 1200 baud
Even Parity
No Echo
Auto Key Repeat
No Parity Error indicate
Display not saved
No flashing characters
Control Characters not displayed

In order to change these parameters, please refer to the software operating specifications.

1.2 OPTION INSTALLATION INSTRUCTIONS

A. RECHARGEABLE BATTERY OPTION

1. Disconnect HT/1000 from any external equipment.
2. Depress OFF button.

3. Loosen the two captive screws at the bottom of the battery access door.
4. Remove battery access door by pulling bottom of door outward, then sliding it toward the bottom of the HT/1000.
5. Carefully remove the six batteries.
6. Replace them with the six enclosed rechargeable cells noting polarity as shown inside of the case.
7. Replace the battery access door by reversing steps 3 and 4.
8. Using a pair of pointed pliers carefully remove and discard the rubber plug from the charger jack at the bottom of the HT/1000.
9. Connect the enclosed charger to the HT/1000 and plug it into a standard wall outlet.
10. Charge the unit for approximately 12-14 hours. Unit may be operated while charging.

WARNING

Never operate unit on charger without batteries installed.

B. CABLE OPTION

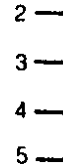
1. Disconnect HT/1000 from any external equipment.
2. Depress OFF button.
3. Loosen the four case mounting screws (non-battery access door screws).
4. Carefully lift off the back of the HT/1000 and set it to the right of the unit, being careful not to damage the wiring connecting the case halves.
5. Remove the old cable by carefully squeezing the tab on the connector while pulling the cable away from the printed circuit board. Hold the black connector firmly in place while removing the cable.
6. Install the enclosed new cable.
7. Carefully replace the back of the HT/1000 making certain that the cable exits through the notch in the bottom of the case.
8. Install the four case mounting screws.

1.3 POWER SAVING TIPS

- 1) When operating from the line power keep V_{in} as close to 5.0 VDC as possible. Anything higher than that is just wasting power that must be dissipated as heat in the HT/1000.
- 2) Operate unit at highest baud rate possible. More power is consumed during data transfers than when unit is idle, therefore keep data transfers as brief as possible. (Doesn't matter in RS-422-A)
- 3) If RTS/CTS are not needed, leave unterminated. Any load on RTS consumes power, and internal circuitry for the HT/1000 CTS circuit allows it to send data to the interfacing equipment (if it's always ready), without any pullups or jumpers on CTS. (Note, this is for RS-232-C only).
- 4) Especially when operating on batteries, turn off unit when it is not being used.
- 5) If possible, operate in "Echo" Mode as data is only sent in one direction for each character as opposed to "No Echo" mode where each character sent by the HT/1000 is both sent and received. (See #2).
- 6) Use the buzzer as infrequently as possible as it consumes a considerable amount of power.

1.4 OFF LINE TEST CONNECTIONS

RS-232-C, RS-422-A, TTL Units



CURRENT LOOP Units

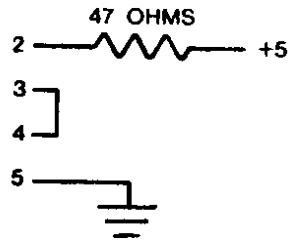


FIGURE 1.1

KEYBOARD OPERATION

2.1 Control Keys

The HT/1000 Unit uses a four by eight (32) keyboard. The keyboard uses 28 keys to generate the 128 ASCII Characters. The 4 keys at the top of the unit are used as function keys. The configuration is shown in Fig. 2.1

Certain keys are used to generate the most commonly used control characters. These keys and an explanation of each key are as follows:

KEY	FUNCTION
LF	Transmits the Line Feed control character (HEX 0A)
CR	Transmits the Carriage Return control character (HEX 0D)
SP	Transmits the ASCII Space character (HEX 20)
BSP	Transmits the Back Space control character (HEX 08)
ESC	Transmits the Escape control character (HEX 1B)
CTRL	Control - This key sets up the control mode of operation. The next key stroke, with the exception of the SPACE key will transmit the control character. If the user depresses the SPACE key the unit looks for a valid control character on the upper right of the keys to be depressed. Once a key is depressed and the character transmitted, the unit will resume normal operation.

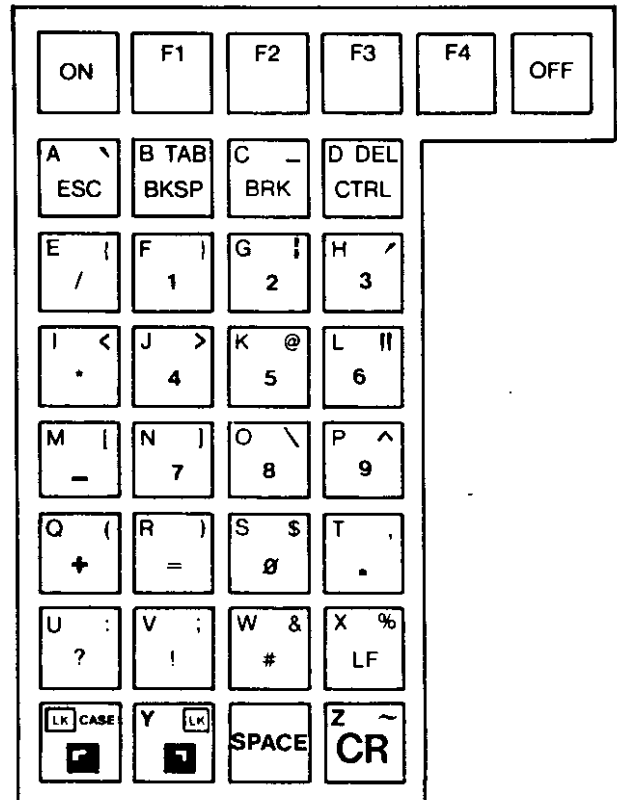


Fig. 2.1 HT/1000 Keypad

NOTE

The ON and OFF keys are only functional when the unit is to be powered by the batteries. Otherwise they are ignored. If the unit is operating on batteries and line power is supplied, the unit will automatically switch over to the line supply. It will turn off when the line power is interrupted.

2.2 SPECIAL FUNCTION KEYS

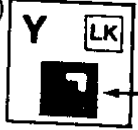
There are two keys in the lower left hand section of the keyboard that are used for special keyboard functions. These functions are as follows:

(Shift Keyboard Left)



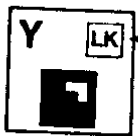
This function will shift the keyboard to the Alpha characters on the top left of each key. After the key is transmitted the keyboard will unshift and resume normal operation.

(Shift Keyboard Right)



This function will shift the keyboard to the punctuation characters on the top right of each key. After the key is transmitted the keyboard will unshift and resume normal operation.

LK



This function is selected when the user depresses the shift right key twice. This function will lock the keyboard into the right shift mode. When selected this function will remain engaged until the user selects the shift right key again, unlocking the shift.

LK



This function is selected when the user depresses the shift left key twice. This function will lock the keyboard into the upper left shift mode for each key. This enables the user to send alpha characters thereafter with only one key stroke. This function, when selected, will remain engaged until the user selects the shift left key again, unlocking the shift.

CASE



This function is selected by depressing the shift right key then depressing the shift left key. This is used to lock in lower case alpha characters until the unlock is depressed. This function will enable the user to send lower case characters with only a single key stroke. This function will remain engaged until the user depresses the shift left key again, unlocking the keyboard.

2.3 FUNCTION KEYS (F1 to F4)

The purpose of the function keys is to enable the user to program special messages that can be transmitted with only a single keystroke. This function utilizes a buffer that is sixteen (16) characters long.

The total number of characters associated with the function keys cannot be more than 16 characters; that is, if F1 contains 5 characters, F2 contains 3 characters, F3 contains 2 characters, then F4 cannot contain more than 6 characters (i.e. $5+3+2+6=16$ characters).

The function keys can contain any ASCII value from Null (HEX 00) to Del (HEX 7F). The function keys can use any combination of control keys (HEX 00 to HEX 1F) and lower or upper case ASCII characters as well as all of the punctuation characters.

The function keys can be programmed manually or on line from a host system.

The function keys are programmed manually on power up when the user simultaneously depresses the "Shift Left Key" and the "Carriage Return Key" (CR) as power is applied. This sequence forces the unit into the program mode, which is described elsewhere.

To program the function keys a menu called "PGM Function Keys" will appear in the KBD Mode of the programming sequence. This menu is described in detail later.

To program the unit while on line, an ESC sequence is used. This escape sequence is explained in the section entitled "Downline Loading".

If the function keys are not programmed each key will assume a single value. These are:

- F1=DC1 (HEX 11)
- F2=DC2 (HEX 12)
- F3=DC3 (HEX 13)
- F4=DC4 (HEX 14)

DISPLAY OPERATION

NORMAL DISPLAY

The normal display is 64 characters on 4 lines. Characters are input starting at the lower left hand corner of the display and after each line feed or, after the line is filled, the display data shifts upward one line at a time. When display data is shifted past the top line, it is lost. If cursor positioning is used, the characters can be set to any position on the display. When the line is full or a line feed is encountered, the cursor will shift down to the next line (if available); if the cursor is at the bottom of the display, the display will scroll up.

The HT/1000 display has seven types of keyboard input modes which are indicated by seven different cursors as shown in Figure 3.1. These are as follows:

3.1 Normal Mode Cursor - - When in the normal mode, the unit will read keys that are in the unshifted position. That is, all of the numeric keys and some of the punctuation keys will be available from the keyboard. The "Normal Mode Cursor" is displayed as a flashing square block.

3.2 Shift Left Mode Cursor - - When in the shift left mode, the unit will read the alpha keys on the keyboard. The "Shift Left Mode Cursor" is displayed as a flashing square block with the upper left corner removed.

3.3 Shift Right Mode Cursor - - When in the shift right mode the unit will read the punctuation characters on the right side of each key on the keyboard. "Shift Right Mode Cursor" is displayed as a flashing square block with the upper right corner removed.

3.4 Control Mode Cursor - - When the control key (CTRL) is pressed, the unit will shift the keyboard left, to access the alpha keys. The control mode cursor appears as "CT".

3.5 Lower Case Mode Cursor - - When the user presses the lower case key (shift right followed by a shift left), the HT/1000 will display the lower case cursor which is signified by the character "LC". This cursor will act similar to the shift left lock function, which locks the keyboard left, except that this function will transmit lower case alpha characters as long as

the keyboard is not unlocked. Pressing the shift left key will unlock the keyboard, the cursor will change to the normal cursor and the keyboard will resume its normal operation.

Characters that are input to the HT/1000 are displayed at the position of the cursor. After each character is input the cursor is incremented to the next location.

3.6 Low Battery Cursor - - This cursor replaces the normal cursor whenever the batteries are in need of replacing or recharging. All other cursors are available to the user.

3.7 Not Clear to Send Cursor - - This cursor replaces the normal cursor whenever the equipment connected to the HT/1000 is not ready to receive data. However the HT/1000 can still receive and display characters.

3.8 Received Characters - - Characters that are input to the HT/1000 are displayed at the position of the cursor. After each character is input the cursor is incremented to the next location.

Control - - If the HT/1000 is not in the "Display Control Characters" mode, then upon receipt of the following characters, the HT/1000 will perform as described.

- CR - Move the cursor to the left most position of the current line.
- LF - Perform a CR, then move cursor down one line. If cursor is already at bottom of screen then move display up one line.
- TAB - Move cursor one position to the right. If cursor is at right most position, do nothing.
- BS - Move cursor one position to the left. If cursor is at left most position, do nothing.
- FF - Clear screen and position cursor to lower left most position.
- BEL - Sound the internal buzzer for about ¼ second.

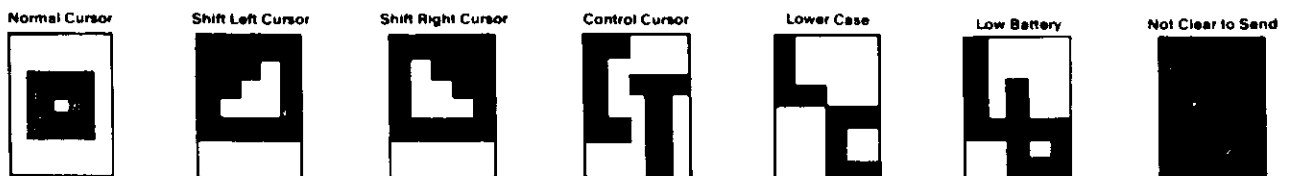


Fig. 3.1 Display Cursors

ESCAPE SEQUENCES

The following escape sequences control the cursor position and the clearing of display characters when transmitted to the HT/1000.

ESC A Cursor Up

Moves the cursor up 1 row of characters. The horizontal position is unchanged. If the cursor is at the top of the display, the cursor will remain unchanged.

ESC B Cursor Down

Moves the cursor down 1 row of characters. The horizontal position is unchanged. If the cursor is at the bottom of the display, the cursor will remain unchanged.

ESC C Cursor Right

Moves the cursor 1 position to the right. If cursor is at the right most position, the cursor will remain at the end of the current line.

ESC D Cursor Left

Moves the cursor 1 position to the left. If cursor is at the left most position, the cursor will remain at the beginning of the current line.

ESC H Home

Positions the cursor at the lower left most position of the display.

ESC J Erase to End of Screen

Erase all characters from the current cursor position to the end of the display. The cursor will remain at the current position.

ESC K Erase to End of Line

Erase all characters from the current cursor position to the end of the current line. The cursor will remain at the current position.

ESC Y (row) (col)

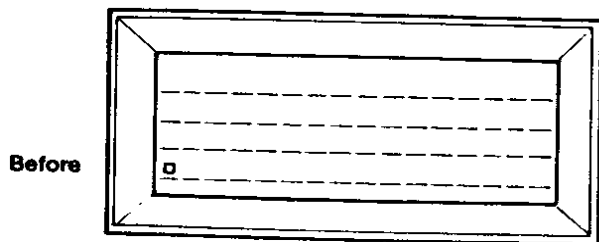
Positions the cursor to anywhere on the screen by using single ASCII characters as defined below in Table 4-1. Absolute cursor positioning (row) and (col) are single ASCII characters as defined below:

Row = SP (HEX 20) to # (HEX 23)
Col = SP (HEX 20) to / (HEX 2F)

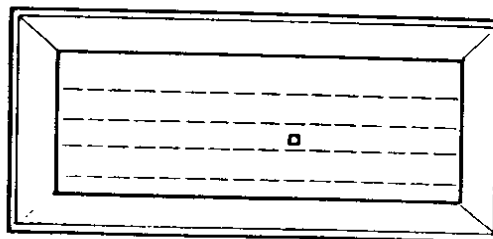
	Column	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ROW	SP	!	"	#	\$	%	&	'	()	*	+	,	-	.	/	
1	SP	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
2	!	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
3	"	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
4	#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Table 4-1

Example:



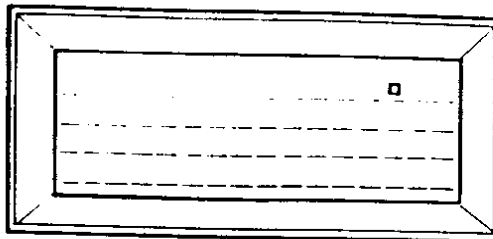
ESC Y ")



The cursor will move to row 3, column 10.

ESC Y sp-

After



The cursor will move to row 1, column 14.

KEYBOARD PROGRAM MODE OPERATION

The HT/1000 provides a keyboard program mode through which the user may set up different parameters to run the HT/1000, such as Baud Rate, Parity, Etc. These parameters may be selected through the keyboard program mode or down line loaded. Parameters selected in this mode are permanently stored. The user starts the program sequence by holding down the shift left key and the carriage return key (CR) simultaneously at power up. The HT/1000 will display "Main Menu" on the top line and the following on the bottom line;

"COM DSP KBD EXT"

which are commands to get the user into various modes of programming.

These commands are as follows:

COM	HT/1000 Communications options (Baud, Parity, Etc.)	19,200
		9600
DSP	HT/1000 Display options (Flashing Char., Etc.)	4800
		2400
KBD	HT/1000 Keyboard options (Auto Key Repeat, Etc.)	1200
		600
EXT	Exit the HT/1000 programming Mode and begin operation	300
		150

The commands at the bottom of the display correspond to the function keys (F1 - F4) that are at the top of the keyboard. Pressing F1 will perform the "COM" function, F2 will perform the "DSP" function and F3 will perform the "KBD" function. Pressing F4 will exit the programming mode and begin normal operation. Each of these functions will be discussed in detail starting with the COM option.

5.1 COM Communications

By pressing the COM (F1) function key the HT/1000 will display the first program of the communications option.

"BAUD RATE"

The HT/1000 will display the message "Baud Rate" on the first line of the display; the second line will display a value, which is the Baud Rate currently selected. The unit defaults to 1200 Baud and this will be the value when the unit is first powered up. The bottom line contains "PRV NXT SAV EXT". These commands will select a value from the appropriate table in memory as follows:

PRV

Selects the previous value to be displayed.

NXT

Selects the next value to be displayed.

SAV

Permanently saves the value presently displayed. After the value is saved, the unit will step to the next mode to be programmed. If the HT/1000 is at the last function to be programmed the unit will return to the "Main Menu".

EXT

Exits the mode that the user is currently in, saves the value displayed and returns to the main menu.

The unit is capable of implementing the following baud rates -

19,200
9600
4800
2400
1200
600
300
150

The Baud Rates are selected by using the "NXT" (F2) / "PRV" (F1) keys on the keyboard. If the user has stepped to 150 Baud the next "PRV" pressed will display "19,200" Baud, and if the user has stepped back to 19,200 Baud the next "NXT" will display "150" Baud.

"PARITY"

The HT/1000 will display the message "Parity" on the top line. The second line will contain the parity default value of "Even". Parity is displayed by using the "NXT"/"PRV" function keys.

The unit is capable of implementing the following Parities -

Even
Odd
Space
Mark

If the user has stepped to mark parity the "NXT" will display "EVEN" parity and if the user has stepped back to even parity the "PRV" key will display "MARK" parity.

"MODE"

The HT/1000 will now display the message "MODE" on the top line and the default value of "NO ECHO" on the second line.

Mode assumes the following values -

ECHO Echo characters to the HT/1000 display as well as transmitting them to the host system. Normally used when host is in half duplex mode.

NO ECHO Do not echo characters to the HT/1000 display, transmit only to the host and assume the host will transmit characters back to the HT/1000. Normally used when host is in full duplex mode.

"DISPLAY PARITY ERROR" - - The HT/1000 will display the message "Display Parity Error" on the top of the display and the default value of "NO" on the second line.

"Display Parity Error" can assume the following values - - -

YES - - - The unit will display "PE" when a Parity Error occurs, and will ignore character with Parity Error.

NO - - - Does Not Display "PE" if parity was incorrect and displays the character received.

"AUDIBLE PARITY ERROR" - - - The HT/1000 will display the message "Audible Parity Err" on the top of the display and the default value of "NO" on the second line.

Audible Parity Error can assume the following values--

YES - - - The unit will ring a bell for approximately 1/4 of a second when a error occurs.

NO - - - Does not ring bell if parity is incorrect.

NOTE: Both "Audible Parity Error" and "Display Parity Error" can be selected at the same time. Thus a user can hear as well as see the error.

5.2 DSP - - - - Display Options

To enter this function, the HT/1000 has to be in the program mode and at the "Main Menu". This function is selected by pressing the F2 key while at the main menu. The HT/1000 will now go through the display functions. The first function is "Flashing".

"FLASHING" - - - The HT/1000 will display "Flashing?" on the top of the display and the default value of "NO" on the second line. Flashing allows the user the option of flashing important messages and/or warning messages to the operator thus enabling the user to quickly notice any errors. Once flashing has been enabled all the user need do is bracket the

statement transmitted to the HT/1000 as follows: precede the statement with the control character "SUB" (Control Z/Hex 1A) and end the statement with the control character "CAN" (Control X/Hex 18). All of the characters between "SUB" and "CAN" will now flash. The user can continuously flash the characters by never transmitting the "CAN" character from the host system.

Flashing cannot be enabled when the "Display Control Characters" option described below is selected.

Flashing can assume the following values:

YES - - - Enable character flashing under the control of host CPU.

NO - - - Does not flash characters

"DISPLAY CONTROL CHARACTERS" - - - The HT/1000 will display the message "DSPLY CTRL CHARS" on the top line and the default value of "NO" on the second line. This option displays all ASCII control characters (HEX 00 to HEX 1F) as a flashing version of the equivalent keyboard character and (HEX 7F) as a left arrow. Therefore, an EOT (Control D/Hex 04) is displayed as a flashing D. The user can distinguish the difference from control characters and normal characters because the control characters will flash at a rate of approximately 2 HZ. This option has priority over the flashing characters option described in the last paragraph. That is, if "Flashing" was selected and display control characters was also selected, then "Display Control Characters" will be the only one used. This allows the user to differentiate between the two options.

"Display Control Characters" can assume the following values:

YES - - - Enables "Display Control Characters" and disables flashing if it was selected. Flash any character below the HEX value of 1F received from the host. Do not perform CR, LF, etc.

NO - - - Does not display control characters. Ignore all control characters except those that are executed by the HT/1000 i.e. LF, CR, BKSP, etc.

"SAVE DISPLAY" - - The HT/1000 will display the message "Save Display?" on the top line and default value of "NO" on the second line. This option, when enabled, will save what is currently on display when it is powered down. The display will be saved in the units battery backup memory. This option gives the user the ability to keep messages on the display overnight, over a weekend, etc. When the unit is powered up, the display that was saved will be redisplayed; if the option was not selected the display will be blank on power up.

Save Display can assume the following values:

YES - - - Enable unit user to save the current display in battery backup memory.

NO --- Do not enable this option. The display is cleared on power up.

5.3 KBD --- Keyboard Operation

To enter this function the HT/1000 has to be in the program mode at the "Main Menu". This function is selected by pressing the F3 function key on the keyboard while at the "Main Menu". The HT/1000 will now go through the keyboard programming functions starting with auto key repeat and is explained in detail as follows:

"AUTO KEY REPEAT" --- The HT/1000 will display the message "Auto Key Repeat" on the top of the display and the default value of "YES" on the second line. This option will allow the user to transmit a key as long as the key is depressed. Once a key is pressed, and after a 1/2 second delay, a character will be transmitted at a rate of 7 characters a second. The characters will continue to be transmitted until the key is released.

"Auto Key Repeat" can assume the following value ---

YES --- Enables auto key repeat, allowing the user to transmit at 7 characters a second as long as the key is held down.

NO --- Does not allow user to continuously transmit; allows only single characters per keystroke.

"MAXIMUM AUTO REPEAT" --- The HT/1000 will display the message "Max Auto Repeat" on the top line of the display and the default value of "YES" on the second line. This option will allow a user to continuously transmit a character once a key is pressed. Once a key is pressed, the HT/1000 will begin transmitting the character under the key, there is no delay as in "Auto Key Repeat" before a key is transmitted. The key will transmit 40 characters a second for baud rates over 300, the unit transmits 15 and 30 characters per second for baud rates 150 and 300 respectively. The unit will continuously transmit until key is released.

"Max Auto Repeat" can assume the following values ---

YES --- Enables "Maximum Auto Repeat". Begin transmitting at 40 characters per second with no delay.

NO --- Does not enable "Max Auto Repeat". Allows only single keystrokes.

NOTE: "Auto Key Repeat" and Maximum Auto Repeat" are mutually exclusive options. The one that is last selected is the mode that is enabled.

"DISABLE KB SHIFT" --- The HT/1000 will display the message "Disable KB Shift" on the top line and the default value of "NO" on the second line. This option lets the user add three more keys (Control, Left Shift and Right Shift) to his keyboard. If this option is selected, the shifted characters above

the keys (alpha and punctuation) cannot be used. (For ease of operator interface, the user may not want to use the shifted characters). The three keys are replaced with the following values:

SHIFT LEFT ---- A

SHIFT RIGHT ---- B

CONTROL KEY (CTRL) ---- C

(Refer to "Special Function Keys" section to help identify these Keys).

"Disable Shift" can assume the following values --

YES --- Disables the Keyboard shift, cannot use the alpha characters or punctuation marks above the keys. Use the default characters.

NO --- Allows shifting of the keyboard to obtain all ASCII characters.

"KEYBOARD AUDIO FEEDBACK" ---

HT/1000 will display the message "Audible Keys" on the top line and the default value of "NO" on the second line. This will let the user select the option of allowing the bell to ring each time a key is depressed.

Keyboard Bell can assume the following values --

YES --- Lets the bell ring when each key is pressed.

NO --- Does not allow bell to ring when each key is pressed.

5.4 "PROGRAM FUNCTION KEYS"

The HT/1000 will display "PGM Function Key" on the top line and "F1" on the second line. The user will also note that the bottom line of the display does not have a "SAV" function. This is because the save function has been moved to the second menu of this option and the user can only exit from this menu. "F1" corresponds to the first function key; "F2", the second function key, etc. The "YES" key that is displayed on the bottom of the display will allow the user to begin operation of programming the function keys. The "NO" key will increment the "F1" on the second line of the display. The "F1" will step to "F2", "F3" and "F4". When the display reads "F4" the next depression of the "NO" key will change the "F4" to an "F1". "Fx" corresponds to which function key the user wishes to program. F1 equals function key F1, F2 equals function key F2, etc. The "EXT" key will return the program to the "MAIN MENU" and the user can program another function or exit from there to the main program flow.

By pressing the "Yes" key, the HT/1000 will enter the function key programming mode. The display will now contain a flashing cursor on the top line, the function key RAM on the second line, 4 up-hats (^) on the third line and four commands on the bottom line. The flashing cursor indicates where the user will start to program the function key that was selected in the previous menu.

The second line displays all of the function key messages currently contained in the function key RAM, the third line contain a series of up-hats(^) which are used as separators for each of the messages. The first function key message is between the start of the display and the first up-hat, the second message between the first and second up-hat, the third message between the second and third up-hat and the fourth message between the third up-hat and the fourth up-hat.

The bottom line contains two editing functions, a SAVE function and and EXIT function. The first two functions are used to edit the function key data the user is altering. "BSP" indicates to backspace a character for each key depression and "FSP" indicates to forward space for each key depression. The "SAV" function will save the contents the user has input on the top line. The contents will be stored in the function key RAM from the first character input to the last character input. The data that remains from the last character to the end of the display will fill in the remainder of the function key RAM. Note that if the user inputs more characters then there is RAM available, the last message could be cut off. If the

user inputs less characters then is available the remainder of the RAM will be filled in with either the remainder of the function key RAM or if there is no data in RAM then it will be filled with blanks.

The "EXT" key will exit this menu and return to the "PGM Function Key" Menu and redisplay the function key "Fx" that was being programmed. The data that the user installed in the HT/1000 will not be entered into the function key RAM. This allows the user to exit, if a mistake was made, without worrying if the function key was programmed with bad data.

When the user presses the "SAV" key, the data displayed is the data saved. The program will return to the "PGM" Function Key" menu and the user can now program another function key or exit back to the main menu.

NOTE: If a key is not programmed it will assume it's default values of:

F1 = DC1 (HEX11)

F2 = DC2 (HEX12)

F3 = DC3 (HEX13)

F4 = DC4 (HEX14)

DOWNLINE LOADING

Many options of the HT/1000 may be selected by downline loading of the proper sequence as described below. These options are permanently stored in memory when selected. They may be altered by downline loading at any time.

Example: ESC(x) (Length) (chars) -- sets-up user definable function keys

IF x = 1 then set-up function key F1
 = 2 then set-up function key F2
 = 3 then set-up function key F3
 = 4 then set-up function key F4

Length = 1 to 16 (16 is total combined characters for all four of the function keys; the length can be broken down to any combination under each of the function keys (F1 - F4) but the maximum is still 16 characters for all of the function keys. The length must be in Hex, (0 to F), with 0 representing 16 and 1 through F representing 1 through 15 respectively.

Chars = Characters (the message for that function key)
 The number of characters transmitted by each key is determined by the length.

Example: The following sequence will program function key F1 to be "TEST?"

ESC 1 5 Test?

Function key F1 will contain the characters "Test?" There will be 11 characters available for the rest of the function keys.

Example: The following sequence will program F1 thru F4.

**ESC 1 5 TEST? ESC 2 2 NO ESC 3 3 YES
 ESC 4 8 TESTING?**

F1 = "TEST?"
 F2 = "NO"
 F3 = "YES"
 F4 = "TESTIN"

Function key F4 contains only the first 6 characters from the original "TESTING?" as the letter "N" was the 16th character.

The default values of these keys can be found in the Section titled "Program Function Keys".

ESC P (10 chars) Sets up communication options and other terminal features. The ten characters which follow ESC P control the terminal features as shown below:

BAUD RATE	= 2 Chars	Defaults	40
KEYBOARD MODE	= 2 Chars	Defaults	01
DISPLAY	= 2 Chars	Defaults	00
SPARE	= 2 Chars	Defaults	00
COMMUNICATIONS	= 2 Chars	Defaults	80

ESC P WWWXXYYZZ

ESC P	<u>VV</u>	<u>WW</u>	<u>XX</u>	<u>YY</u>	<u>ZZ</u>
	BAUD RATE	KEYBOARD MODE	DISPLAY	SPARE	COMMUNICATIONS LINE CONTROL

All of the ESC P characters must be programmed together. Unlike the function keys, they cannot be individually programmed.

NOTE: All values programmed are affected as soon as the characters are transmitted with the exception of Baud Rate, which becomes effective at the next Power Down/Power Up Sequence.

See Tables 1 through 4 in Appendix A for the character values to use for the desired options.

To program the keyboard, display, and communications values, refer to Appendix A.

The following is an example of a typical downloader instruction:

EXAMPLE: ESC P 40012000C1

ESC P	<u>40</u>	<u>01</u>	<u>20</u>	<u>00</u>	<u>C1</u>
	BAUD RATE	KEYBOARD MODE	DISPLAY	SPARE	COMMUNICATIONS LINE CONTROL

This sequence will setup the unit for the following:

1200 BAUD
AUTO KEY REPEAT
NO ECHO
KEYBOARD SHIFT ENABLED
NO FLASHING CHARACTERS
CONTROL CHARACTERS DISPLAYED
ODD PARITY
NO AUDIO FEEDBACK
NO PARTY ERRORS DISPLAYED
AUDIBLE PARITY ERROR INDICATE
DISPLAY NOT SAVED
NO MAX AUTO REPEAT

* **NOTE:** When initiating the downline loading command, both the host and terminal must be at the same baud rate and parity.

7

SELF TEST

The HT/1000 performs three separate self tests at every powerup to verify integrity. These tests are a display test, a nondestructive internal memory test (to verify the microprocessor's memory is functional) and a ROM sum check test (to verify the unit has not lost any of its ROM Data). Each are described in detail as follows:

7.1 DISPLAY TEST - The HT/1000 runs a display test to verify that all of the dots are functional. The HT/1000 runs a series of characters through the display, the first is a pound sign (#) followed by an "M" and ending with the character "I". This requires a visual check by the user to verify that all of the dots are functional.

7.2 NONDESTRUCTIVE INTERNAL RAM TEST - The microprocessor contains 128 Bytes of internal RAM that is used for display buffering, flags, counters and function key messages. All of the RAM is utilized for this function and some of the memory cannot be changed once the unit has been programmed. During the self test the unit will read a Byte of data from RAM, complement it, write the data back to the same memory location, read the data back from the same location, complement it again and verify it against the original data for accuracy. The unit will store its original value at the same location, and reread it. The value should be the same. If the values ever differ from each other, the HT/1000 will display a memory error message on the display.

7.3 CHECKSUM TEST - The HT/1000 performs a sum check of the ROM that contains the program. This is done by reading each of the ROM locations and adding it to a register. (The carry is not added). Once the addition is done the value is compared against the original valued stored. If this value is different the internal memory of the ROM has been altered and the unit is not functioning properly. The HT/1000 will display a ROM checksum error if the unit fails this test.

After all of these tests are run and the unit detects no errors the unit will respond with a small flashing square in the lower left hand corner of the display. This is the HT/1000 cursor and normal operation can now begin.

7.4 RESET BUZZER - During the self test the HT/1000 buzzer will turn on. If it does not do this, or if it does not cease at the end of the self test, then consult the Trouble Shooting section in Appendix B.

IMPORTANT: To change the programmed options, the user must depress and hold **CR** and **Shift Left Keys** simultaneously through the self-test period. Otherwise, the unit will operate using the last set of options stored in memory.

8.1 BATTERIES:

A) Low Battery Indicator.

The normal cursor will change to a flashing LB character when batteries are in need of recharging or replacing. The alkaline cells should have about 10% of useful life at this time, while the rechargeable cells should have less than 5% of useful life left. Refer to figure 8.1 for battery life. Refer to Figure 8.2 for dimensions of the Battery charger.

One way to have longer battery operation is to install mercury cells. Available from Electronic distributors, they have about 40% longer operating life than alkaline cells. When the LB cursor appears they have less than 3% of useful life left. They are available as ZM9 from Duracell, E9 from Eveready, and T9 from Ray-O-Vac.

B) SHELF LIFE

The self life of a battery is drastically affected by storage temperature. However at normal room temperature, typical shelf life is as follows:

TYPE	TIME TO 90% CAPACITY
ALKALINE	4 years
MERCURY	2 years
NICKEL CADMIUM	2 weeks

NOTE

The high quality, industrial Ni Cad batteries have an expected life of 1000 charge/discharge cycles, and, in most circumstances, will not require replacement more often than every five years.

C) BACK UP BATTERY

There is an internal battery, not replaceable by users, that maintains information in the internal memory. This battery should have a typical useful life of about 10 years. Should the display ever show the message BAD BACKUP BATT, contact the factory for instructions.

WARNING

Use only the Termiflex charger (P/N 51-0014-000), as it has been specifically designed to fulfill the requirements of the HT/1000. Use of any other may cause permanent damage to the HT/1000 and will void your warranty.

Power Requirements/Battery Life

	Power Supply Current (Typical)	Battery Life (Hours)	
		Alkaline	Ni-Cad (Option)
RS-232-C	9mA	190	55
RS-422	16mA	107	32
Current Loop	7mA	244	72
TTL	6mA	284	84

Figure 8.1

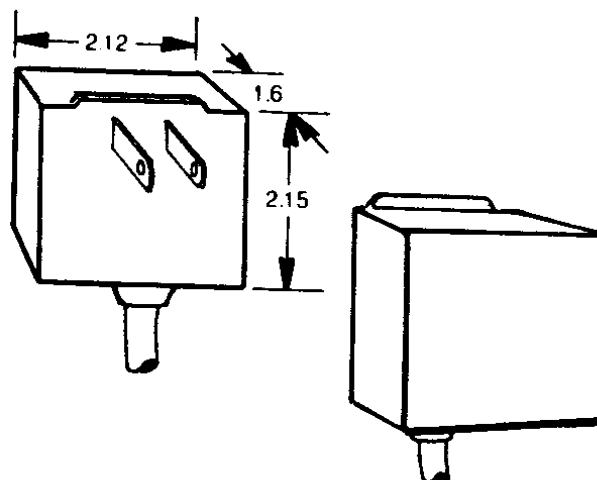


Figure 8.2 BT/100 Charger Basic Case Size Dimensions

8.2 HT/1000 INTERFACE THRESHOLDS

	INPUT		OUTPUT	
	MARK	SPACE	MARK	SPACE
RS232	-15.0V to + 0.5V	+1.4 to + 15.0 @ 2mA	-5.0 to -15.0	+5.0 to +15 @ 3mA
RS422	-0.20V to - 6.0V	+0.2 to +6.0 @ 3mA	-2.0 to -5.0	+2.0 to +5.0 @ 40mA
TTL	0.0 V to + 0.5V	+1.4 to +5.2 @ 0.1mA	+0.00 to +0.7	+2.4 to +5.2 @ 2mA
20mA C.L.	5. to 25mA	0. to 2.5mA @ 150V	15 to 25mA	0. to 2.5mA @ 150V

8.3 HT/1000 INTERFACE PIN ASSIGNMENTS

CONNECTOR				SIGNAL NAME			
MODULAR	DB 15	DB 25	9PIN CIR	RS-232	TTL	20mA C.L.	RS-422
1	BLU	7	7	7	GROUND	GROUND	GROUND
2	YEL	2	2	2	XMIT DATA	XMIT DATA	LOOP OUT
3	GRN	3	3	3	RCV DATA	RCV DATA	LOOP IN
4	RED	4	4	4	TFX RDY	N/C	LOOP OUT RTN
5	BLK	5	5	5	CLR TO SEND	N/C	LOOP IN RTN
6	WHT	15	9	9	POWER	POWER	POWER

For more information on RS-232-C or RS-422-A interfaces,
refer to the respective Electronic Industries Association Standards.

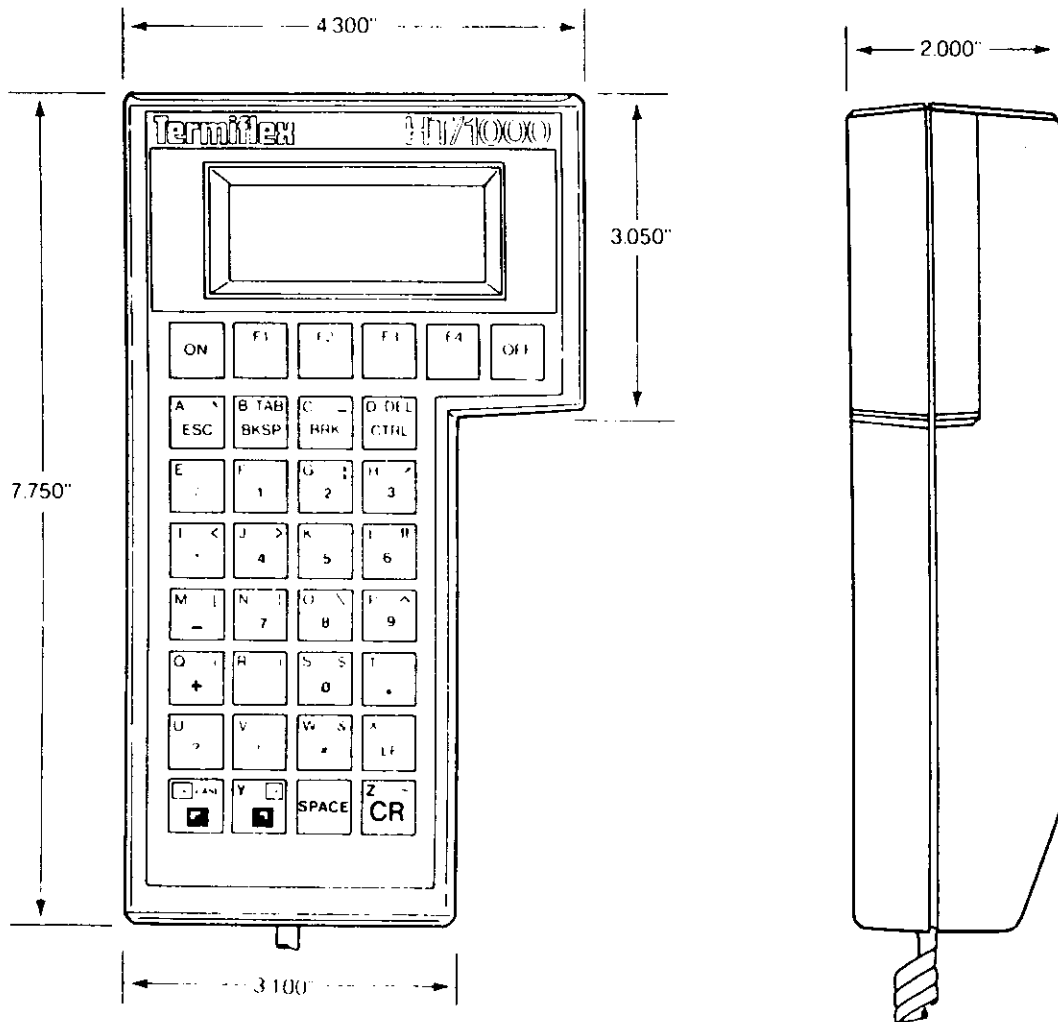


Figure 8.3 HT/1000 Outline Drawing

8.4 MECHANICAL

Weight	- 24 oz. (680g)
Cable Length	- 6 feet (1.8m)
Case Connector	- 6 pin modular jack: AMP 520250-3
Cable Connector	- 25 pin, DB-25P

8.5 ENVIRONMENTAL

Operating Temperature Range	- 0°C to +50°C
Storage Temperature Range	- -20°C to +70°C
Humidity	- 95% non-condensing
Intrinsic Safety	- Contact Factory

8.6 PARITY

There are only four possible parities. They are commonly referred to as, Odd; Even; Mark; & Space, or Odd; Even; & 8 bit, No parity; & 7 bit, No parity. Each set is identical and Termiflex literature conforms to the former nomenclature. A brief description of each type of parity follows:

- ODD:** The total number of bits set to a logical "1" in an ASCII character is examined. If it is odd, the parity bit is cleared (0). If it is even, the parity bit is set (1) thereby making the total number of "1" 's ODD.
- EVEN:** The total number of bits set to a logical "1" in an ASCII character is examined. If it is even, the parity bit is cleared (0). If the total is odd, the parity bit is set (1) thereby making the total number of "1" 's EVEN.
- MARK:** The parity bit is always set (1).
- SPACE:** The parity bit is always cleared (0).

The parity bit is the eighth or most significant bit in the data word is as illustrated in Fig.8-4.

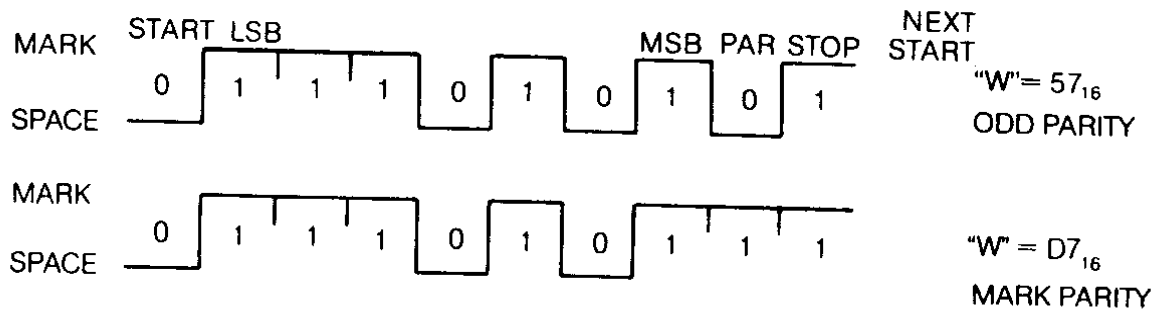


Figure 8-4

8.7 CABLE LENGTHS

When discussing cable lengths two different areas should be examined:

- Power Cable
- Communication Cable

A) The power cable's length is limited primarily by the voltage drop per foot of the cable. Therefore, for the HT/1000, a typical drop per 1000 feet is as follows:

WIRE GAUGE	DIAMETER	VOLTAGE DROP/1000 FEET
22 (19/34)	(.67 mm)	.70 V/1000 Ft. (304m)
24 (19/36)	(.50mm)	1.05 V/1000 Ft. (304m)
26 (19/38)	(.33mm)	1.72 V/1000 Ft. (304m)

Therefore if you are supplying power from 1000 feet away from the HT/1000 and using 24 gauge wire, you must supply a minimum of 5.8VDC at the source to meet the 4.75V min requirement of the HT/1000. (4.75V + 1.05V = 5.8 V)

B) The communication cable's maximum length is a function of interface, baudrate, and cable capacitance. Typical Values are listed below for 19,200 BPS.

RS-232-C	50 Ft	15M
RS-422-A (W/O termination resistance)	1000 Ft	304M
RS-422-A (termination resistance = 100ohm)	4000 Ft	1220M
TTL	25 Ft	7.5M
20mA. C.L.	(1)	(1)

1) The 20mA. C.L. interface is also a function of compliance voltage and as such is listed in table 8-1.

2.0m A. C.L. Ideal maximum cable lengths at 19200 baud

COMPLIANCE VOLTAGE	ALPHA #1178 22 GUAGE (.67mm) 7/30 22.6pf/ft	ALPHA #5016 24 GUAGE (.5mm) 7/32 20.8pf/ft
5	875 (269m)	950 (292m)
20	215 (66m)	225 (69m)
45	95 (29m)	100 (31m)
145	25 (8m)	30 (9m)

TABLE 8-1

NOTE

1) Compliance Voltage = Applied Voltage -Active Drops.

2) Recommended Usage of Interfaces.

The TTL interface is recommended for use in low noise environments where interconnections can be kept short.

RS-232-C Should be used where only short runs can be used but moderate noise immunity is required.

RS-422-A Can be used over long distances with high noise immunity

20mA Current Loop can be used over long distances with very good noise immunity and the added advantage of electrical isolation.

APPENDIX A

TABLE 1 - BAUD RATE CHARACTER STRING

BAUD RATE	CHARACTER STRING
19200	00
9600	10
4800	20
2400	30
1200	40
600	50
300	60
150	70

TABLE 2 - KEYBOARD OPTIONS CHARACTER STRING

OPTION					
ECHO CHAR ENABLED	KB SHIFT DISABLED	KB AUDIO ENABLED	MAX KEY REPEAT	AUTO KEY REPEAT	CHAR STRING
				X	01
			X		02
			X	X	03
		X			04
		X		X	05
		X	X		06
		X	X	X	07
	X				08
	X			X	09
	X		X		0A
	X		X	X	0B
	X	X			0C
	X	X		X	0D
	X	X	X		0E
	X	X	X	X	0F
X					80
X				X	81
X			X		82
X			X	X	83
X		X			84
X		X		X	85
X		X	X		86
X		X	X	X	87
X	X				88
X	X			X	89
X	X		X		8A
X	X		X	X	8B
X	X	X			8C
X	X	X		X	8D
X	X	X	X		8E
X	X	X	X	X	8F

TABLE 3 - DISPLAY OPTIONS CHARACTER STRINGS

OPTION			
FLASHING CHARS ENABLED	DISPLAY CONTROL CHARS ENABLED	SAVE DISPLAY ENABLED	CHAR STRING
			00
		X	08
	X		20
	X	X	28
X			80
X		X	88
X	X		A0
X	X	X	A8

TABLE 4 - COMMUNICATIONS OPTIONS CHARACTER STRINGS

TYPE OF PARITY	DISPLAY PARITY ERROR ENABLED	AUDIO PARITY ERROR ENABLED	CHAR STRING
SPACE			00
SPACE		X	01
SPACE	X		02
SPACE	X	X	03
MARK			40
MARK		X	41
MARK	X		42
MARK	X	X	43
EVEN			80
EVEN		X	81
EVEN	X		82
EVEN	X	X	83
ODD			C0
ODD		X	C1
ODD	X		C2
ODD	X	X	C3

APPENDIX B

TROUBLE SHOOTING

SYMPTOM

If there is no display or beep @ power-up	go to step_1
If beep @ power-up does not stop	go to step_2
If display shows "Ram Error"	go to step_2
If display shows "Rom Error"	go to step_2
If display flashes "Bad Backup Battery"	go to step_2
If cursor remains a large black block	go to step_3
If interfacing equipment does not receive characters	go to step_4
If unit doesn't receive characters	go to step_5
If display shows garbled message	go to step_6
If display shows double characters	go to step_7
If beeper sounds or ^P E is displayed with incoming characters	go to step_8

STEP	PROBABLE CAUSE	TO SOLVE	IF SOLVED	IF NOT SOLVED
1	Bad power Connection	Operate Terminal on battery power	Check Power and ground connections and voltage level.	Go to 11
2	Bad Reset	Turn off power wait 5 sec., then then turn on	Continue using terminal	Go to 11
3	No clear to send	Install a self-test connector (fig. 1.4)	Be sure pin 5 is high by either leaving it open or shorting 4 to 5	Check the connections on the HT/1000 connector.
4	Bad Xmit connections	Put terminal in local echo mode, check baud rate & parity, then depress keys	Go to 11	If the Terminal displays characters but still does not transmit then go to step 9
5	Bad Recv. connections	Check parity & baud rate. Send data from interfacing equipment	If terminal displays characters, continue using terminal	Go to step 9
6	Incorrect baud rate	Set baud rate & parity to be compatible with interfacing equipment	Continue using terminal	Go to 11
7	Terminal is set for "echo" in a "no echo" application.	Set Terminal to "no echo" mode	Continue using terminal	Go to 11

STEP	PROBABLE CAUSE	TO SOLVE	IF SOLVED	IF NOT SOLVED
8	Incorrect Parity	Set Parity of terminal to be compatible with interfacing equipment	Continue using terminal	Go to 11
9	Bad I/O connection	Install a self test connector, Fig. 1.4, depress keys	Go to 10	Check connections on the HT/1000 I/O connector
10	Bad I/O connections on interfacing equipment or incorrect control signals	If being used, check RTS, CTS, DTR on interfacing equipment. Voltage levels should be ± 3 to ± 15 VDC	Check I/O connections of all control signals and data lines. If 20 ma. current loop is being used, then check current loop sources.	Get control signals to the proper level by the use of jumpers.
11	Defective Equipment	Call Factory		



DIGI-DATA CORPORATION

8580 Dorsey Run Road, Jessup, Md. 20794 • (301) 498-0200 • TWX (710) 867-9254

Model 70R
RS-232 C COMPATIBLE
TAPE CARTRIDGE SYSTEM
OPERATION MANUAL

0553525-0000

revA110983

DIGITAL TAPE UNITS • • • DIGITAL SYSTEMS

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1 - INTRODUCTION AND INSTALLATION

1.1 SCOPE OF MANUAL. This manual describes the Model 70R, RS-232 Compatible Cartridge Tape System manufactured by Digi-Data Corporation, 8580 Dorsey Run Road, Jessup, MD 20794. 70R Tape Systems consist of a cartridge drive and an interface board mounted in a desk-top chassis. This document describes each component of the 70R system with special emphasis on the RS-232 interface board. After a general description of the equipment and directions for installation, this manual explains all relevant RS-232 I/O signals, 70R tape format and all tape operations. This manual then describes the protocol for issuing commands from the computer and receiving status from the drive. An appendix explains how to disassemble the system, change options on the interface board, and replace the individual components.

1.2 REFERENCE DOCUMENTS. The following documents include more information about aspects of system operation which this document does not describe in detail.

Cartridge Drive Operation Manual, Digi-Data Corporation.

Unrecorded Magnetic Tape Cartridge for Information Interchange, 0.250 inch (6.30 mm), 1600 bpi (63 b/mm), Phase Encoded, ANSI No. X3.55-1977.

EIA RS-232-C -- Interface between data terminal equipment and data communication equipment employing serial binary data interchange.

1.3 DESCRIPTION OF EQUIPMENT.

1.3.1 CARTRIDGE DRIVE. The cartridge tape drive reads and records high density data on cartridges mechanically conforming to ANSI X3.55-1977. (Note that 70R Systems accept 450' and 555' cartridges as well as the 300-foot cartridge described in this specification.) Data is recorded serially on four tracks. For more detailed information, including specifications, recording codes and maintenance procedures, see the cartridge drive operation manual.

1.3.2 DESK TOP CHASSIS. The desk top chassis contains the power supply for the cartridge drive. The drive mounts on the chassis front panel. The front panel also contains the cartridge loading slot, three indicator lights and one pushbutton Rewind switch. The indicators connect to the cartridge drive Options Connector and are described briefly below. (See the cartridge drive manual for a pinout of the Options Connector and complete descriptions of all of the signals.)

1) SELECT: This indicator lights when the cartridge drive is selected (i.e. being addressed).

2) BOT: This indicator lights when the loaded cartridge is physically positioned at or before the Load Point Sensed (LPS) tape hole (logical BOT). (See the cartridge drive manual for more information on cartridge format and tape zones.)

3) SAFE: This indicator lights when the SAFE switch on the loaded cartridge is in the file protected position, thus preventing writing or erasing.

1.3.3 RS-232 INTERFACE BOARD. The RS-232 interface board is microprocessor controlled. It enables the cartridge drive to communicate with a computer or other controller via a standard EIA RS-232 interface port. The interface board decodes serial input sequences to generate the appropriate cartridge drive command lines, and encodes cartridge drive status lines to communicate the required information to the host over the serial line. The board also formats data records as described in chapter 3 of this manual and generates or checks parity on all data bytes. During data transfers, incoming data is loaded into a record-sized buffer until the entire record has been transmitted. The interface board then transfers the data to the cartridge drive, which records it on tape.

In addition to the microprocessor, the design includes 49 integrated circuits. Switch-selectable setups include parity (odd, even, or none), number of stop bits (1, 1½, or 2), and baud rate (75 to 19,200 baud or external clocking to 175k baud).

1.4 INSTALLATION. 70R Tape Systems are shipped already configured to your order. To install the system, simply attach a standard RS-232 cable to the I/O at the back of the chassis (upper right hand corner) and plug in the power cord. If you wish to change any of the options at any time, see Appendix A, figure A-6.

1.5 SPECIFICATIONS.

Operating Environment	40° to 115° F (5° to 45°C) (cartridge limited) Altitude to 10,000' (3000m) 20% to 80% Relative Humidity (non-condensing)
System Size	5.2 in (13.2 cm) H x 8.95 (22.7) W x 14.7 (37.3) D
System Power Requirements	99 to 132 VAC @ 1.5 A or 198 to 264 VAC @ .75 A; 49 to 400 Hz
Cartridge Drive Tape Format	4 track serial: Unidirectional (6410/8310) or Bidirectional (6420/8320); 6400 bpi IMPM (6410/6420) or 8333 bpi IMPM (8310/8320)
Transfer Rate	Up to 192K bits per second (64xx Series drives) Up to 312.5K bits per second (83xx Series drives)
Interface Board	
Controller to Interface:	True (0) = +3 to +25 VDC False (1) = -3 to -25 VDC
Interface to Cartridge Drive	True = 0.0 to +0.6 VDC False = +2.5 to +5.0 VDC
Interface, internal	True = +2.5 to +5.0 VDC False = 0.0 to +0.7 VDC
Power	+5 VDC @ 2.5A max. +18 VDC @ 50mA max. -18 VDC @ 50mA max.

2 - RS-232 INTERFACE

2.1 INTRODUCTION. The RS-232 serial interface transfers data and control signals between the tape system and a host computer or modem. This chapter describes the physical and electrical characteristics of the serial interface, defines relevant signals, and describes RS-232 data format. It also explains cabling both directly to a host computer and to a modem.

2.2 INTERFACE CONVENTIONS. All Digi-Data 70R Tape Systems are fully RS-232 compatible. The interface cable connects to the tape system via a standard 25 pin D-subminiature female connector with all relevant signals located on the proper pins. See figure 2-2.

True (Space, or binary 0) is indicated by +3 VDC to +25 VDC; false (Mark, or binary 1) is indicated by -3 VDC to -25 VDC.

RS-232 transfers data asynchronously and therefore requires an accurate clock. Baud rates may be set on the board or the host can supply an external clock via the RxC and TxC lines. Figure 2-1 illustrates the proper data format. The default state for the data lines is Mark. To signal the beginning of a data character, a single Start bit (Space) at the appropriate baud rate precedes the data. On the eight bit cycles following the Start bit come the eight data bits in the byte, least-significant-bit (LSB) first. If selected, a parity bit follows the most-significant-bit (MSB) of the byte. After the last bit of the byte, whether parity or the MSB, the data line returns to the Mark state for one, one-and-one-half, or two cycles; these cycles are called the Stop bits. Another Start bit precedes the next data byte or, after the last byte of the record, the line remains high.

2.3 CABLING. Shielded data cables must be provided by the user in Radio-Frequency Interference (RFI) sensitive applications. The shield braid of the cable should be attached to the chassis through the jack screw connection at each end of the cable.

70R Tape Systems will use different cables depending on whether they are connected directly to the host computer or to a modem. The two types of cables are described below.

2.3.1 DIRECT CABLES. When cabled directly to a computer 70R Tape Systems only require three I/O signals: Signal Ground, Transmitted Data and Received Data. Note that Transmitted Data from each component must be connected to Received Data from the other. This will require cross-wiring the connector if your system does not perform the crossover internally. If it does, straight-through cables similar to those used with modems will be required. Protective Ground may be connected (depending on applicable safety specifications) but has no effect on the interface. If your system is configured for an external clock, RxC and TxC must also be connected. RxC (External Receiver Clock) and TxC (External Transmitter Clock) are generated by the host system. They clock data at a rate of one clock per bit. Data must be valid on the rising edge of the clock. See figures 2-2 and 2-3.

2.3.2 MODEM CABLES. Modem cables are wired straight-through with no cross-wiring since the modem performs all crossovers internally. The cable must include Transmitted Data, Received Data, Signal Ground, Request to Send, Clear to Send, Data Set Ready, Received Line Signal Detector and Data Terminal Ready. See figure 2-2.

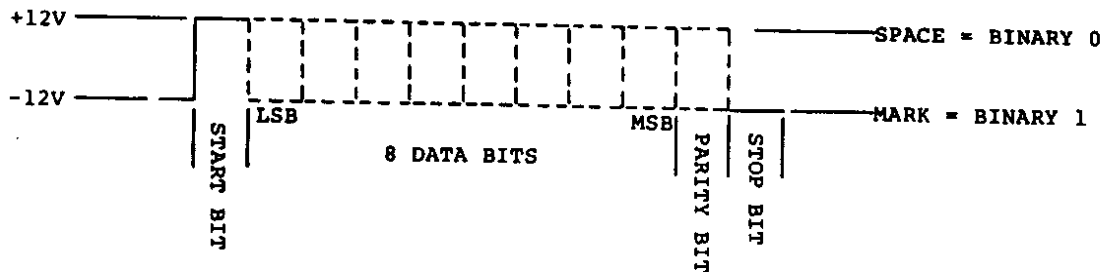


Figure 2-1, Data Format

NAME: Protective Ground PIN: 1 EIA NAME: AA DIRECTION: Common USAGE: All
REMARKS: Provides the interface with Protective Ground which is attached to the desk top chassis and the power cord ground as a safety feature to prevent shock.

NAME: Transmitted Data (TD) PIN: 2 EIA NAME: BA DIRECTION: Output USAGE: All
REMARKS: Outputs data from the interface board. It is in the Mark state when no data is being transmitted.

NAME: Received Data (RD) PIN: 3 EIA NAME: BB DIRECTION: Input USAGE: All
REMARKS: Inputs data to the interface board. It is in the Mark state when no data is being received.

NAME: Request to Send (RTS) PIN: 4 EIA NAME: CA DIRECTION: Output USAGE: Modem
REMARKS: Signals to the modem that the interface has data ready for transmission. The modem should respond with CTS when prepared to receive data from the interface.

NAME: Clear to Send (CTS) PIN: 5 EIA NAME: CB DIRECTION: Input USAGE: Modem
REMARKS: Indicates to the interface that the modem is ready to receive data. The interface board will not transmit data unless CTS is true. If CTS is dropped in the middle of a transmission, the interface will finish transmitting the current character and then stop transmission.

NAME: Data Set Ready (DSR) PIN: 6 EIA NAME: CC DIRECTION: Input USAGE: Modem
REMARKS: Indicates that the modem has established a telephone connection. The interface board will not transmit or receive data when DSR is false.

NAME: Signal Ground PIN: 7 EIA NAME: AB DIRECTION: Common USAGE: All
REMARKS: Establishes the common reference ground for all RS-232 signals. It is connected to the tape system power supply; it is also connected to Protective Ground.

NAME: Rec'd Line Signal Detector (RLSD) PIN: 8 EIA NAME: CF DIR: Input USAGE: Modem
REMARKS: Indicates that the modem is ready to transmit data to the interface. The interface board will not accept data if this signal is false. Also known as Data Carrier Detect (DCD). The interface should respond with DTR.

NAME: External Transmitter Clock (TxC) PIN: 15 EIA NAME: DB DIR: Input USAGE: All
REMARKS: Clocks TD when the baud rate switches are set for external clocking. TxC is generated by the device receiving the data. The clock rate equals the baud rate. Data is shifted out on the mark-to-space transition of each pulse.

NAME: External Receiver Clock (RxC) PIN: 17 EIA NAME: DD DIRECTION: Input USAGE: All
REMARKS: Clocks RD when the baud rate switches are set for external clocking. RxC is generated by the device transmitting the data. The clock rate equals the baud rate. Data is shifted in on the mark-to-space transition of each pulse.

NAME: Data Terminal Ready (DTR) PIN: 20 EIA NAME: CD DIRECTION: Output USAGE: Modem
REMARKS: Indicates to the modem that the interface is ready to receive data. DTR comes true in response to RLSD.

Figure 2-2, 70R Interface Connector Signals

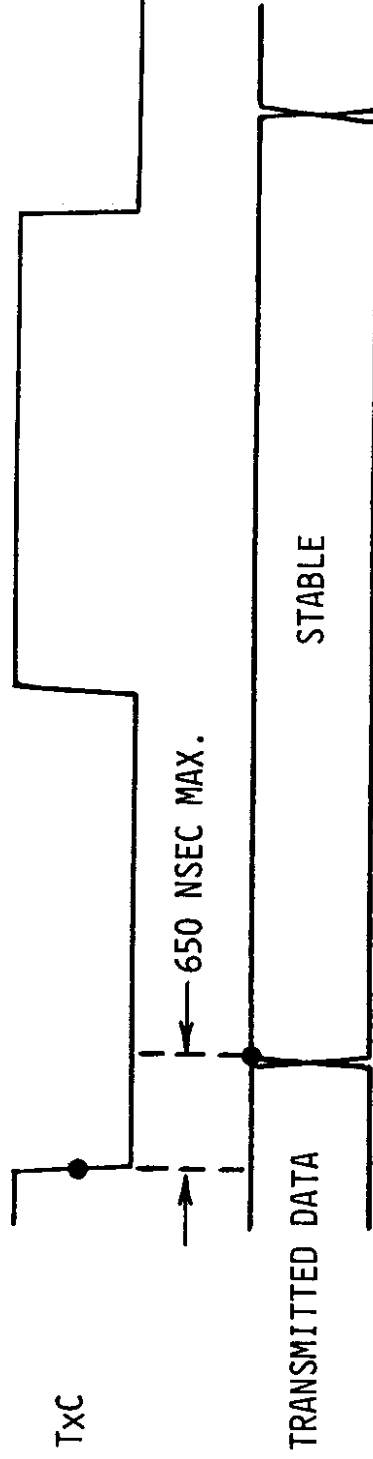
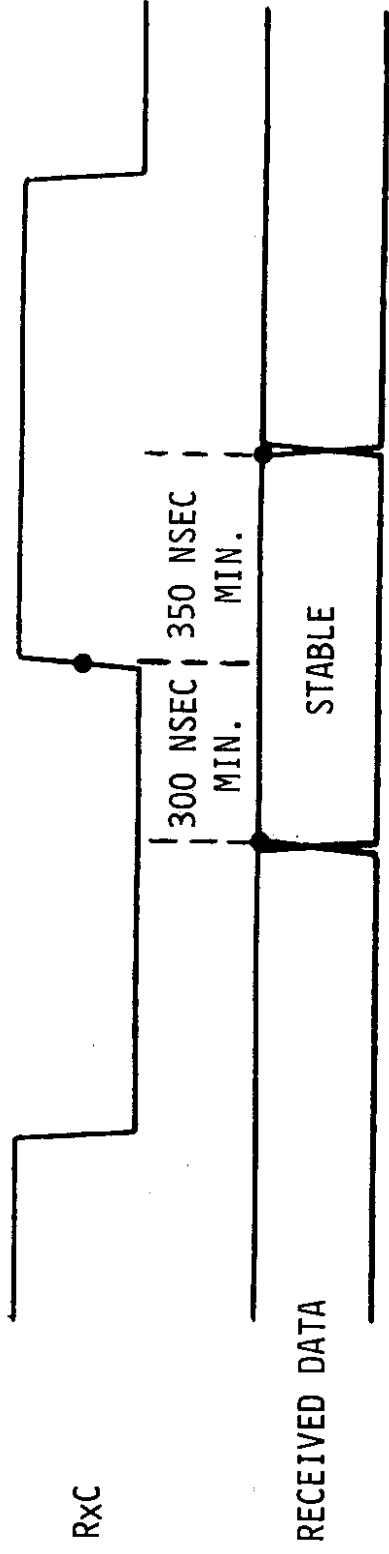


Figure 2-3, Data/Clock Timing

3 - TAPE OPERATIONS

3.1 INTRODUCTION. This chapter describes all 70R tape operations. It discusses tape and record format, then explains the sequence of events in each operation. (For more information on these operations at the drive level, see the Cartridge Drive Manual. For information on the cartridge's specifications, see ANSI Specification no. X3.55-1977.)

3.2 RECORD FORMAT.

3.2.1 DATA RECORDS. See figure 3-1 during the following discussion of data record format.

PREAMBLE + PRESYNC	Five 00 hex bytes followed by 08 hex byte
-----	-----
SYNC BYTE	FF hex
-----	-----
RECORD TYPE BYTE	22 hex = Data
-----	-----
DATA	Number of bytes determined by record length given in MA
-----	-----
LRCC BYTE	Even parity bit-wise of data
-----	-----
RECORD TYPE BYTE	22 hex = Data
-----	-----
POSTAMBLE SEQUENCE	01 hex byte followed by five 00 hex bytes
-----	-----

1.25" nominal (1.2" Minimum) Interrecord Gap

Figure 3-1, Data Record Format

All records begin with a preamble. The preamble enables the read circuits to synchronize on the data before decoding. 70R preambles consist of five 00 hex bytes followed by 08 hex. All bytes, including data, are recorded least-significant-bit first, followed by an even parity bit. After the preamble, the software records the Sync Byte (FF hex) and the Record Type Byte (22 hex for data records or 55 hex for filemarks).

Immediately following the record type byte comes the data. The number of bytes in the data block is specified in the Mode Argument (MA). See paragraph 4.3.1. Note that the MA must specify a quantity less than or equal to the length of the buffer on the interface board or data errors will result. See the descriptions of Read and Write operations below for more details.

The Longitudinal Redundancy Check Character (LRCC) byte follows the data. The LRCC is formed from the even horizontal parity of bits 0 to 7 of each byte in the data portion of the record (i.e. the even parity of bit 7 in each data byte is bit 7 in the LRCC, the even parity of bit 6 in each data byte is bit 6 of the LRCC, etc.). Only data bytes are used to calculate the LRCC; the Preamble, Record Type byte and Sync bytes are ignored. Note that although the LRCC will contain a parity bit, this bit is generated from the vertical parity of the LRCC itself rather than from the horizontal parity of all the data parity bits. When writing, the LRCC is generated in software before actually writing the data. During read or read-after-write operations, the LRCC is regenerated in hardware and compared to the LRCC recorded on tape.

After the LRCC, the Record Type Byte (22 hex) is repeated, followed by the postamble (01 hex followed by five 00 hex bytes).

3.2.2 FILEMARKS (EOF RECORDS). End-Of-File records begin with the same preamble and Sync Bytes as data records. They continue with a Record Type Byte (55 hex), followed immediately by a postamble identical to that of data records. See figure 3-2.

PREAMBLE + PRESYNC	Five 00 hex bytes followed by 08 hex byte
-----	-----
SYNC BYTE	FF hex
-----	-----
RECORD TYPE BYTE	55 hex = Filemark
-----	-----
POSTAMBLE SEQUENCE	01 hex byte followed by five 00 hex bytes
-----	-----

1.25" nominal (1.2" Minimum) Interrecord Gap

Figure 3-2, Filemark Format

3.2.3 RECOMMENDED TAPE FORMAT. Most 70R operations do not require a special tape format beyond the record format described above and the restrictions imposed by the cartridge (legal recording area, etc.). The Off Line Copy operation, however, requires two consecutive EOF records at the end of data on each track. If the filemarks are missing, the operation will not recognize the end of data and will run to the End-Of-Tape hole, causing an abort. We therefore recommend that you perform two Write File Mark operations immediately after writing data records to tape. If you wish to add more data to a track after writing the two filemarks, you must overwrite at least the second EOF record or the Off Line Copy operation will not find the data following the second filemark. We also recommend initializing tapes by writing two filemarks on the beginning of each track before performing any operations. When you wish to record a track, start at the beginning and overwrite the filemarks, remembering to rewrite them when your write operation(s) are complete. If a track does not contain data and does not begin with two filemarks, the Off Line Copy operation will abort.

Note that although they are not required, following these conventions also facilitates Record Search Under Mask and Space Forward Records operations.

3.3 TAPE OPERATIONS. This section describes the sequence of events for each tape operation performed by the 70R Tape System. It focuses especially on the signal flow to and from the interface board.

3.3.1 READ OPERATIONS. The read operation reads a block of data from tape and transmits it to the host. The length of the block is encoded in the Mode Argument (MA). See paragraph 4.3.1. The RS-232 interface board takes the record sent by the cartridge drive, strips off all the "formatting" bytes (i.e. all bytes preceding and following the data) and loads the data into its buffer. When the entire record has been loaded, the interface transmits the Drive Status (DS) and Interface Status (IS) bytes to the host (see section 4.4), followed by the data.

If the record on tape is an EOF, the interface does not transfer any data. It signals the host that it has read a filemark by setting bit 6 of the DS byte true. See paragraph 4.4.1.

If the actual length of the record is not the length indicated in the MA, the interface will not transfer any data. It will end the operation and inform the host of the error by setting the Command Status bits in the IS byte (bits 5 and 4) to abort (10).

If an error occurs during a read operation, the interface will backspace over the error record and will attempt to reread it. If the reread is successful, the interface ends the operation normally. If the reread is unsuccessful, the interface will keep trying to read the record correctly. If after a total of 10 attempts read errors still occur, the interface will end the operation and inform the host of the error by setting the Command Status bits in the IS byte (bits 5 and 4) to abort (10).

3.3.2 WRITE OPERATIONS. Write operations transfer data from the host to tape. The length of the block is encoded in the Mode Argument (MA). See paragraph 4.3.1. The RS-232 interface board loads the incoming data from the host into an on-board buffer. When the entire data block has been loaded, the interface board formats it as described in paragraph 3.2.1 and transmits it to the drive, which records it on tape.

The read circuitry in the system is still active during write operations. The interface uses the read-after-write data to check that the record was written correctly. As the read data comes from the drive, the interface regenerates the LRCC in hardware. It also checks the parity bits and monitors the DAD (Data Detected) line from the cartridge drive for dropouts. (DAD envelops the read data; if a dropout occurs, DAD will go false. See the cartridge drive manual for more information.) At the end of the record, if there were no LRCC or parity errors and no dropouts, the interface ends the operation and sends the Drive Status (DS) and Interface Status (IS) bytes to the host. See section 4.4. If an error is detected and if the auto-rewrite on error facility is enabled (i.e. if bit 5 of the Command Argument is 0; see paragraph 4.3.3), the drive will backspace over the error record, erase three inches of tape (thereby erasing the error record), and attempt to write the record again. If the rewrite contains an error, the drive backs up, erases an additional three inches of tape, and tries a third time. The system will rewrite the record up to 10 times. If errors still persist, the system will abort the operation and send the DS and IS bytes to the host. The Command Status bits in the IS byte (bits 5 and 4) will indicate an abort (10). If any of the write attempts is successful, the operation will end normally.

If a write error occurs but bit 5 of the Command Argument (CA) is set, thus disabling the auto-rewrite on error, the interface will terminate the operation after the first attempt and indicate an abort in the Command Status bits of the IS byte (i.e. bits 5 and 4 will be set to 10).

If the number of bytes to be transferred exceeds the length of the buffer on the RS-232 interface board, the drive will write all of the characters in the buffer on tape. It will then pad the data block with FF hex until the number of bytes specified in the Mode Argument are recorded. This will cause a read-after-write error: the LRCC on tape was generated from the entire data block (buffer length plus the excess data), but the LRCC generated during reading is from the buffer-length data plus the FF "padding".

Note that when reading the record on tape, the record length in the MA of the read operation must equal the record length in the MA of the write operation that wrote that record. We recommend using a constant record length for all data transfer operations to help prevent aborts due to faulty MAs. Also, if it is necessary to edit a record (i.e. to rewrite a record in the middle of other records without disturbing the surrounding data), keeping the record length constant will help prevent the edit operation from disrupting the following record. (Note that when editing, bit 5 of the CA should be set to disable the auto-rewrite on error.)

3.3.3 WRITE FILE MARK. Write File Mark operations write an End-Of-File record on tape. The file marks are generated in software on the RS-232 interface board, so no write data is transferred from the host.

To enable the Off Line Copy operation to function properly, two file marks must be written at the end of data on each track (and at the beginning of unrecorded tracks) as described in paragraph 3.2.3, Tape Format. To facilitate this, the Write File Mark command may be executed after the EWS bit (DS bit 2) is set. Note that if you write consecutive EOF records in the middle of a track, the Off Line Copy operation will not copy anything beyond the second file mark. See paragraph 3.3.8.

3.3.4 SPACE RECORDS. The Space Records operations move the tape in the specified direction (forward or reverse) over a number of records equal to the value stored in the Positional Argument (PA) plus 1. That is, the PA range is 0 to 255; the number of records spaced is 1 to 256. If an EOF record is encountered while spacing, the operation terminates and the Command Status bits of the Interface Status (IS) byte (bits 5 and 4) indicate an abort (10). If you follow the tape format described in paragraph 3.2.3, the Space Forward Records operation will abort normally at the end of each track since the drive will encounter a filemark. Otherwise, the drive will continue spacing to the EOT tape hole (or the BOT tape holes on tracks 2 and 4 of bidirectional [or serpentine] drives; see the cartridge drive manual). When the drive reaches EOT (BOT), it will halt immediately and the drive's BUSY signal to the interface board will go false. This will terminate the operation and set the Command Status bits of the IS byte to Abort.

3.3.5 SPACE FILES. These operations are identical to the corresponding Space Records operations except that they space over file marks rather than records. These operations obviously do not abort on EOF. If the drive reaches EOT (BOT if bidirectional), it will halt immediately and the drive's BUSY signal to the interface board will go false. This will terminate the operation and set the Command Status bits of the Interface Status (IS) byte (bits 5 and 4) to Abort (10).

3.3.6 HIGH SPEED SPACE OPERATIONS. These operations are identical to the corresponding low speed operations except that they are executed at high speed. During High Speed Space Records operations, if the PA equals 0, 1 or 2 (i.e. the drive is to space 1, 2 or 3 records), the interface will automatically execute the operation at low speed. All High Speed Space Files operations are performed at high speed, however. Note that if the system encounters an EOF while performing a High Speed Space Records operation, it will abort. Since the deceleration ramp is longer for high speed than for low speed, the drive will overshoot the interrecord gap into the next tape record. Therefore, whenever a High Speed Search Records operation is aborted because of a filemark, we recommend performing a low speed space file operation in the opposite direction to position the tape properly before proceeding.

3.3.7 SEND CURRENT STATUS. This operation causes the interface to send Drive Status (DS) and Interface Status (IS) bytes to the host as soon as the selected cartridge drive is ready. If this operation is commanded with bit 6 of the Command Argument (CA) set, the drive will rewind and halt at BOT before the interface sends the Status Words.

3.3.8 OFF LINE COPY. The Off Line Copy operation makes a duplicate of a cartridge. You must have two daisy-chained cartridge drives (see the cartridge drive manual) to perform this operation. The source drive must be addressed as unit 1 and the destination drive as unit 2.

When the operation begins, the interface reads the first record on track 1 of the source tape. It checks the length of this record and assumes that all subsequent records will be the same length. The interface then writes the record to drive 2 and reads the next record from drive 1. It copies this record to drive 2, and repeats the procedure until it encounters a file mark.

When the interface detects a file mark on the source tape, it performs a Write File Mark operation to drive 2, then reads the next record on the source tape. If this is a data record, it is copied normally. If it is a second file mark, however, the interface assumes that the two file marks indicate the end of a track. After writing a second file mark on drive 2, the interface increments the track on drive 1 and performs a rewind-then-read operation. When this record is stored, it increments the track on drive 2 and performs a rewind-then-write operation. The Off Line Copy then continues normally on the new track.

When the drive reaches two consecutive file marks on track 4, it rewinds both tapes and ends the operation.

The reread-on-error (paragraph 3.3.1) and rewrite-on-error (paragraph 3.3.2) facilities are usually both active during Off Line Copy. (If bit 5 of the Command Argument (CA) is set, the rewrite-on-error facility is disabled.) Note that if there is a write error, the three inch erased gap produced during the rewrite procedure may push drive 2 past the EWS tape hole before drive 1 passes EWS. If this should happen, when drive 1 attempts to copy the next data record to the same track, an illegal command will occur (a write operation while EWS is true), terminating the Off Line Copy operation.

3.3.9 RECORD SEARCH UNDER MASK. This operation searches the tape for a file beginning with a particular data pattern. This data pattern, or mask, may be up to 512 bytes long. If the mask is less than the full 512 bytes, the end of the mask must be marked with BF hex. (Note that if this byte is used within the mask the interface board will interpret it as the end of the sequence and will ignore subsequent characters.) The mask is sent to the interface board immediately following the Command Argument (CA) and is loaded into the interface board buffer. Note that ASCII question marks (3F hex) are "wildcards"; they match any other single character.

The interface begins reading the tape (after rewinding if bit 6 of the CA is set) and loading each record into the read data buffer. It compares the first bytes of each record with the mask. If the loaded record does not begin with the mask bytes, it is flushed and the next tape record loaded. When a record is found that does begin with the mask, that record is transmitted to the host as in a read operation. After transmitting the record, the interface ends the operation. Note that if several records begin with the mask bytes only the first record encountered will be identified and transferred during this operation. If a file mark is encountered before finding a matching record, the operation ends and the Command Status bits in the Interface Status (IS) byte (bits 5 and 4) are set to Abort (10).

4 - COMMUNICATING WITH THE 70R TAPE SYSTEM

4.1 INTRODUCTION. This chapter explains how the host and the 70R Tape System interact. Section 4.2 gives an overview of the system I/O sequence during tape operations. Sections 4.3 and 4.4 describe the Input (Command) and Output (Status) Words in detail. See the cartridge drive manual for a description of the drive to interface board I/O.

4.2 I/O SEQUENCE. The operation begins with a one or three byte input sequence plus write data when appropriate. Three byte protocol consists of the Mode Argument (MA) which specifies the data record size, the drive selection, and the track selection; the Positional Argument (PA) which specifies the count to be used by space commands; and the Command Argument (CA) which is the actual instruction. Each of these bytes is described in detail in section 4.3. One byte protocol, consisting only of the CA, may be used when the MA and PA remain the same as in the preceding operation. The interface uses bit 7 of the first byte to arrive to determine whether the command follows three byte or one byte protocol: if the bit is a 1, then the input follows three byte protocol since bit 7 of the MA is always 1; if the bit is a 0, the input follows one byte protocol since bit 7 of the CA is always 0.

During Write and Search Under Mask operations, the host sends the input data immediately following the CA.

The host awaits the interface's response after sending the command sequence and data (if required). When the drive completes the tape operation, the interface sends the two Status Words: Drive Status (DS) which reports the status of the currently selected drive; and Interface Status (IS) which reports the command status, and the currently selected drive and track. These two words are described in detail in section 4.4.

After successful Read and Search Under Mask operations, the read data follows the IS byte.

4.3 INPUT (COMMAND) WORDS. This section defines each bit of the three Input (Command) Words accepted by the RS-232 interface board. The bytes are transmitted with bit 0 (least-significant-bit) first.

4.3.1 MODE ARGUMENT (MA).

Bit	
7	Must be 1 to distinguish 3 byte protocol from 1 byte protocol (CA begins with 0)
6	Data Record Size*
5	000 = 1024 bytes
4	001 = 2048
	010 = 3072
	011 = 4096
	100 = 8192
	101 = 512
	110 = 8208
	111 = 3630
3	Drive Selection
2	00 = Drive 1
	01 = Drive 2
	10 = Drive 3
	11 = Drive 4
1	Track Selection
0	00 = ANSI track 1
	01 = ANSI track 2
	10 = ANSI track 3
	11 = ANSI track 4

*Must be less than or equal to interface buffer length or errors will result.

4.3.2 POSITIONAL ARGUMENT (PA).

Bit 7 - 0 Used for Space commands. Contains one less than the number of files or records to be spaced -- values 0 to 255 correspond to 1 to 256 files or records.

4.3.3 COMMAND ARGUMENT (CA).

Bit	
7	Must be 0.
6	1 = drive rewinds before executing operation; 0 = drive executes operation from current tape position.
5	1 = Edit mode (disable auto-rewrite on error) 0 = Standard mode
4	Reserved (may be either 0 or 1).
3-0	Commands
0000	Rewind if Bit 6 = 1; Retransmit block if Bit 6 = 0
0001	Read
0010	Write
0011	Write File Mark
0100	Space Forward Records*
0101	Space Forward Files
0110	Space Reverse Records*
0111	Space Reverse Files
1000	Send Current Status
1001	Off Line Copy
1010	Undefined, sets Illegal Command status (see paragraph 4.4.2)
1011	Record Search Under Mask*
1100	High Speed Space Forward Records*
1101	High Speed Space Forward Files
1110	High Speed Space Reverse Records*
1111	High Speed Space Reverse Files

*Aborts on File Mark

4.4 OUTPUT WORDS. This section defines each bit of the two Output (Status) Words transmitted by the RS-232 interface board. The bytes are transmitted with bit 0 (least-significant-bit) first.

4.4.1 DRIVE STATUS (DS). All bits are high true.

Bit	
7	Always 1.
6	File Mark detected.
5	Drive rewinding.
4	Power On and Cartridge in Place.
3	BOT (Tape is positioned at logical Beginning of Tape).
2	EWS (Early Warning Sensed). Indicates that the cartridge is positioned at or beyond the first Early Warning tape hole. Only Write File Mark, Rewind, or Space Reverse operations may be started when this bit is set.
1	FLAG. Indicates that the tape has been rewound since the last operation.
0	Write Enabled. This indicates that the tape is not "SAFE" (not File Protected), thus permitting write operations.

4.4.2 INTERFACE STATUS (IS).

Bit		
7	Always 1	
6	1 = Data follows 0 = No data follows	
5	Command Status	00 = Successful operation
4		01 = Illegal Command*
		10 = Abort**
		11 = Syntax or Parity Error
3	Current Drive	(Should parallel MA bits 3 and 2)
2		
1	Current Track	(Should parallel MA bits 1 and 0)
0		

*Illegal commands include:

- 1) Space Reverse at BOT or Space Forward at EOT
- 2) Any write operation on a File Protected cartridge
- 3) Forward operation (except Write File Mark) past EWS tape hole***
- 4) Any operation to a drive without a cartridge installed
- 5) Setting CA bits 3 - 0 equal to 1010

**Abort indicates that a legal command was loaded and execution begun, but some error caused it to end prematurely. Since tape may have moved before the operation was rejected, unless you know the exact reason for the abort and are certain of the tape position, the next command should be executed relative to BOT (i.e. CA bit 6 = 1).

***Note that if the drive should ever reach true EOT due to a series of re-written filemarks, no more forward motion will be performed whether a complete EOF record is written or not. This situation generates an abort condition.

APPENDIX A - TROUBLESHOOTING AND COMPONENT REPLACEMENT

A.1 INTRODUCTION. This appendix explains how to remove and replace the major components in the desk top chassis. See the cartridge drive manual for further information on servicing the drive.

A.2 OPENING THE DESK TOP CHASSIS.

- 1) Disconnect the AC supply from the chassis.

WARNING! Electric shock hazard from power supply components will be present if the power cord is not disconnected from the AC supply.

- 2) Open the chassis by removing the six screws (3 on either side of the enclosure) and lifting the top off the chassis.

A.3 CARTRIDGE DRIVE.

A.3.1 REMOVAL.

- 1) Unplug the Power Supply cable from the drive's Power Connector (right hand side of the drive as seen from the front panel). See figure A-1. Note the orientation. Do not disconnect the Power Board end of the cable.
- 2) Unscrew the four screws holding the cartridge drive to the front panel. Place the drive face down in the chassis.
- 3) Carefully remove the cartridge drive I/O cable and the front panel cables from the Control Board. Lift the drive out of the chassis.

A.3.2 REPLACEMENT.

- 1) Attach the front panel cable to the Options Connector of the cartridge drive. See the cartridge drive manual for the location of the Options Connector.
- 2) Plug the I/O cable into the drive I/O connector, with pin 1 toward the center of the board. See figure A-2.
- 3) Attach the drive to the front panel using the hardware removed earlier. Note that the enclosure is built either for the standard or for the alternate mounting configuration. All 6403 drives use the alternate configuration, along with any drives whose model numbers are suffixed with a "T." All other drives use standard mounting. Drives of one configuration will not mount directly in enclosures built for the other; you may obtain correct replacement mounting brackets from the factory.
- 4) Attach the cable from the Power Supply Board to the drive's Power Connector, orienting it properly. (Refer to the cartridge drive manual if necessary.)
- 5) Replace the cover of the chassis, securing it with the six screws removed above.
- 6) Plug in the AC power cord from the desk top chassis.

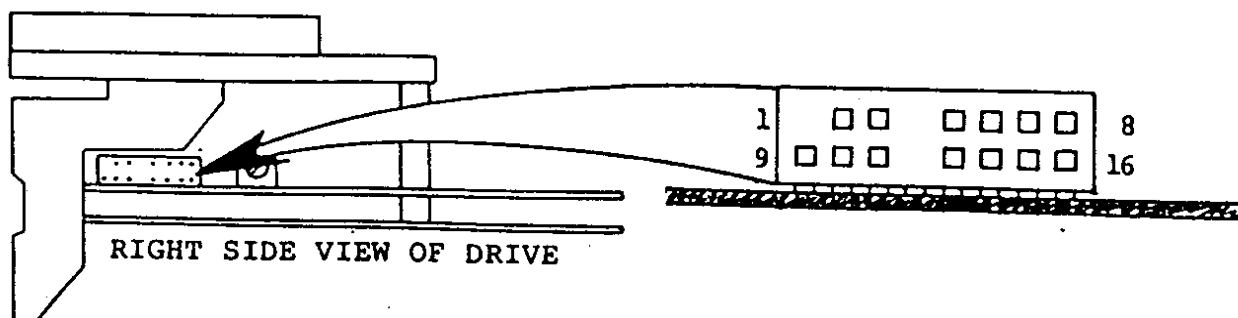


Figure A-1, Drive Power Connector

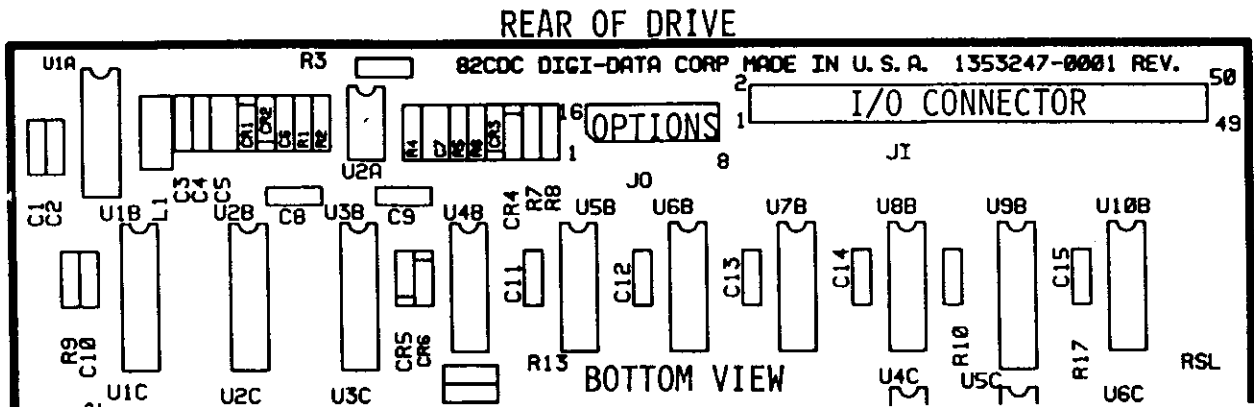


Figure A-2, Options and I/O Connectors

A.4 POWER BOARD.

A.4.1 FAULT ISOLATION. If either the drive or the interface board loses one of its voltages, use the following procedure to determine which device is at fault.

WARNING! This procedure involves opening the chassis with power connected, producing a shock hazard. Only qualified maintenance personnel taking proper safety precautions should perform this procedure. Hazard exists at filter connections, at AC power inputs and at the voltage range switches.

- 1) Unplug the affected device's power cable from the Power Board. Note orientation.
- 2) Plug in the AC power cord from the chassis.
- 3) Check the Power Board output pins for the proper voltages. See figure A-4.

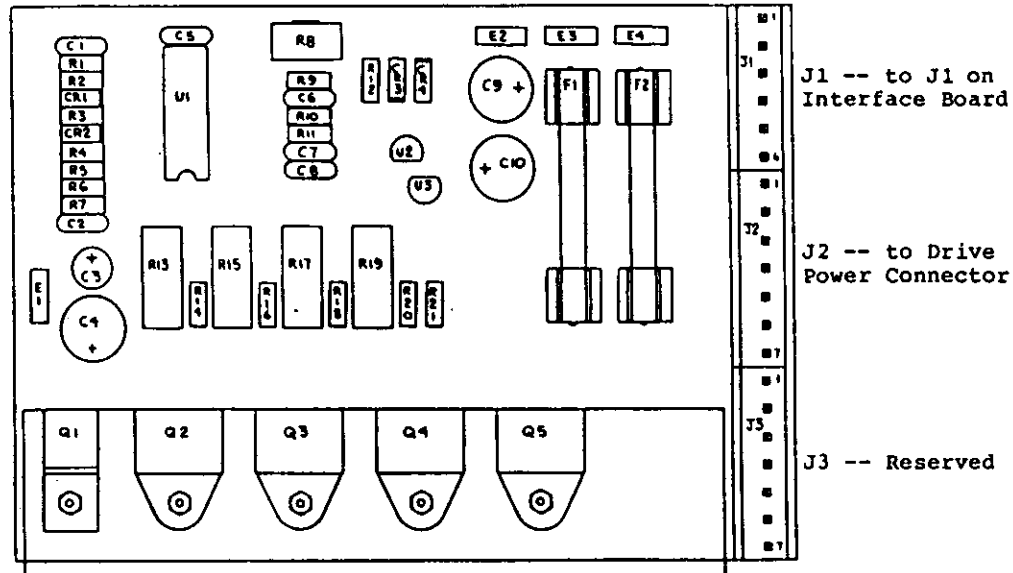


Figure A-3, Series 70 Power Supply Board Connector Locations

J1		J2		J3	
PIN	VOLTAGE	PIN	VOLTAGE	PIN	VOLTAGE
1	+18/+27	1	+18/+27	1	+18/+27
2	-18/-27	2	-18/-27	2	-18/-27
3	GND	3	GND	3	GND
4	+5V	4	+5V	4	+5V
5	GND	5	+5V	5	+5V
6	GND	6	GND	6	GND
		7	GND	7	GND

Figure A-4, Power Board Output Connector Pinouts

4) If the proper voltages are present on the Power Board, the problem is either with the cable or with the disconnected device. Otherwise, check the fuses on the Power Board. If one has burned open, replace it with a Bussman 3A Fast-Blo fuse or the equivalent. If both fuses are intact, replace the Power Board as described in paragraph A.4.2 and A.4.3.

A.4.2 REMOVAL.

- 1) Label and disconnect the four quick-disconnect plugs from the Power Board. See Figure A-3.
- 2) Unscrew the two screws holding the Power Board to the chassis. Lift the board out of the chassis.
- 3) Unplug the drive's Power Connector and the RS-232 Interface Board Power Connector from the Power Board. See figure A-3.

A.4.3 REPLACEMENT.

- 1) Place the Power Board in position in the chassis and replace the screws to hold it to the chassis.
- 2) Replace the quick disconnect connectors from the transformer in their proper locations.
- 3) Plug in the AC power cord from the chassis.

WARNING!

While the chassis is open and plugged in, shock hazard exists. Do not touch capacitor connections, AC power inputs or voltage range switches.

- 4) Connect a DVM to one of the +5V pins and one of the ground pins on the output connectors (see figure A-4). Adjust potentiometer R8 to obtain +5V ±0.05V.
- 5) Disconnect the DVM and unplug the power cord from the desk top chassis.
- 6) Connect the drive and interface board power connectors disconnected in step 3, Removal. Be sure to connect them in the proper locations on the Power Connectors of the Power Board. See figure A-3.
- 7) Replace the cover of the chassis, securing it with the screws removed earlier.
- 8) Plug in the AC power cord from the desk top chassis.

A.5 RS-232 INTERFACE BOARD.

A.5.1 REMOVAL.

- 1) Unplug the Power Supply cable from the interface board's power connector.
- 2) Unscrew the two jack screws holding the interface board to the rear of the chassis. Carefully lift the board from the chassis.
- 3) Disconnect the cartridge drive I/O cable from the interface board.

A.5.2 CONFIGURATION. A single DIP switch on the lower right hand side of the board sets all options. Using a screwdriver, pencil, or your fingernail, set the switches as desired. See either the silkscreen or figure A-6.

A.5.3 REPLACEMENT.

- 1) Check that the desired options are selected on the interface board switches. See paragraph A.5.2.
- 2) Attach the cartridge drive I/O cable to the interface board connector.
- 3) Place the interface board in position in the chassis. Be sure to seat the board in the guides on the bottom of the chassis. Replace the jack screws, connecting it to the chassis.
- 4) Reconnect the power connector to the interface board.
- 5) Replace the cover of the chassis, securing it with the screws removed earlier.
- 6) Plug in the AC power cord from the desk top chassis.

STOP BITS.

1 Stop Bit	-	-	SW1= off	SW2= on
1.5 Stop Bits	-	-	SW1= on	SW2= off
2 Stop Bits	-	-	SW1= on	SW2= on

PARITY.

Odd Parity	-	-	SW3= off
Even Parity	-	-	SW3= on

Should the Interface check parity?

No	-	-	-	-	SW4= off
Yes	-	-	-	-	SW4= on

BAUD RATE.

					SW5	SW6	SW7	SW8
External Clock	-	-	-	-	off	off	off	off
75	-	-	-	-	off	off	off	on
110	-	-	-	-	off	off	on	off
134.5	-	-	-	-	off	off	on	on
150	-	-	-	-	off	on	off	off
300	-	-	-	-	off	on	off	on
500	-	-	-	-	off	on	on	off
1200	-	-	-	-	off	on	on	on
1800	-	-	-	-	on	off	off	off
2000	-	-	-	-	on	off	off	on
2400	-	-	-	-	on	off	on	off
3600	-	-	-	-	on	off	on	on
4800	-	-	-	-	on	on	off	off
7200	-	-	-	-	on	on	off	on
9600	-	-	-	-	on	on	on	off
19200	-	-	-	-	on	on	on	on

Figure A-6, Configuration Switch Settings

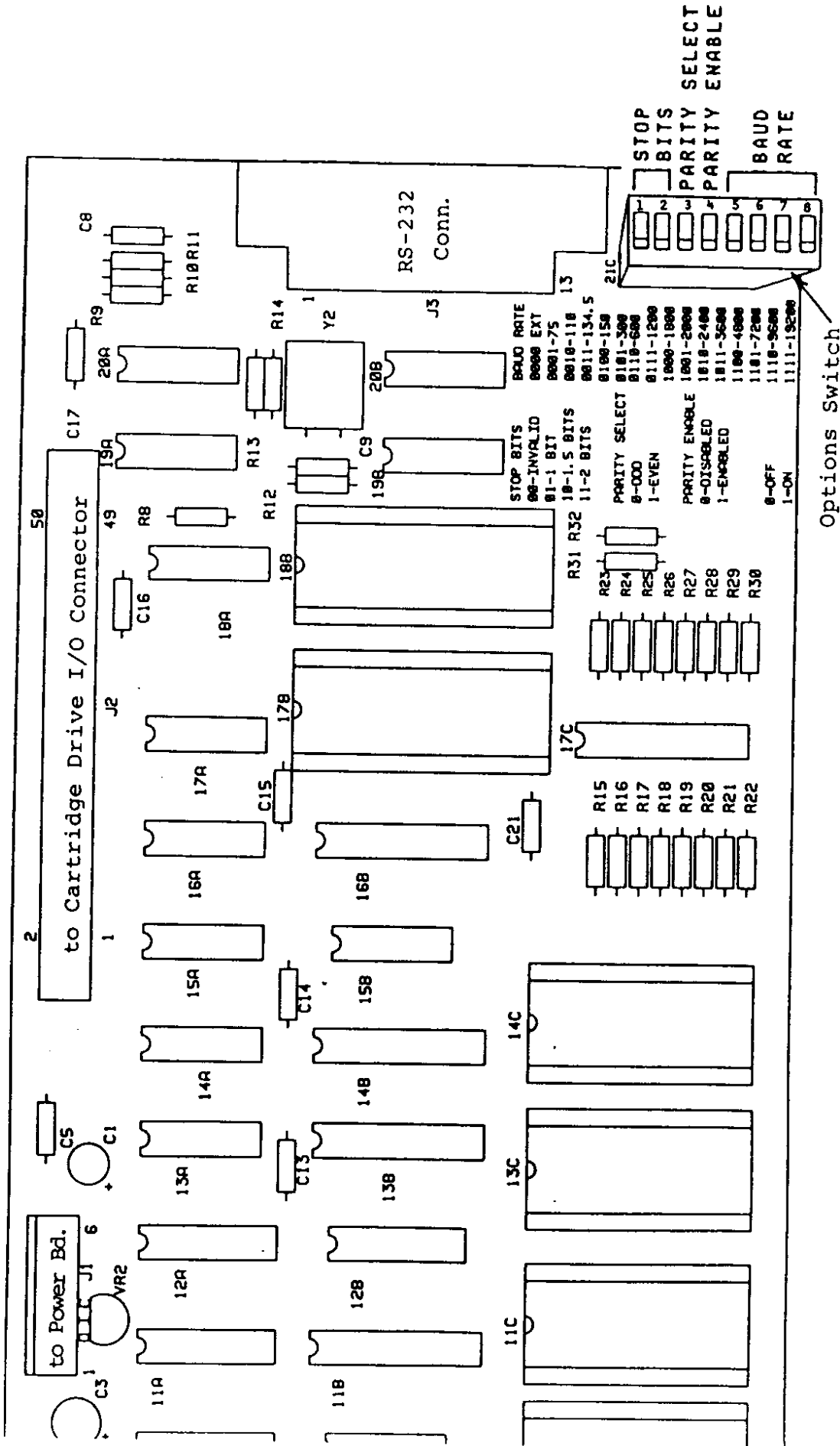


Figure A-5, Right Side of Interface Board

APPENDIX B - MAINTENANCE

The drive's head is the only component which comes in direct contact with the tape. A dirty tape head can cause data dropouts and errors during read and write operations. Periodic cleaning assures that dirt or oxide buildup will not interfere with adequate contact and hence data reliability. The following routine should be performed after every eight hours of system use or every week if the system is not used regularly.

- 1) Remove the cartridge.
- 2) Moisten a cotton swab with isopropyl alcohol or a commercial head-cleaning solvent. Excessive liquid is not required.

CAUTION DO NOT use carbon tetrachloride or any abrasive or hard object. Use of these will damage the head. Spray type head cleaners are not recommended.

- 3) Clean the head thoroughly using firm vertical and horizontal strokes.

CAUTION Use reasonable care when cleaning the head. The delicate tach encoder disk is near the head (just above the capstan). While the disk does have a protective shield, it is possible to slip off the head and damage the disk. A damaged disk will result in motor speed variations.

- 4) Once cleaned, allow time for the solvent to evaporate before loading a tape cartridge.



DIGI-DATA CORPORATION

8580 Dorsey Run Road, Jessup, Md. 20794 • (301) 498-0200 • TWX (710) 867-9254

½-INCH TAPE CARTRIDGE DRIVE

Models 6410, 6420, 6430, 6440

Models 8310, 8320, 8330, 8340

OPERATION AND MAINTENANCE MANUAL

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1) GENERAL INFORMATION

1.1 SCOPE. This manual describes how to install, interface, operate and maintain the start/stop cartridge drives designed and manufactured by Digi-Data Corporation, 8580 Dorsey Run Road, Jessup, Maryland 20794, USA. The models covered are described in Figure 1.1.

MODEL NUMBER	30 IPS LOW DENSITY	37.5 IPS HIGH DENSITY	SERPENTINE	LOW POWER
6410	X			
6420	X		X	
6430	X			X
6440	X		X	X
8310		X		
8320		X	X	
8330		X		X
8340		X	X	X

Figure 1.1, Digi-Data Cartridge Drive Models

1.2 GENERAL DESCRIPTION. Digi-Data Cartridge drives read and record Inverted Modified Frequency Modulation (IMFM) data on cartridges mechanically conforming to ANSI specification X3.55-1977. IMFM data is recorded serially on four tracks by a read-after-write head. Cartridge interchangeability with other Digi-Data cartridge drives depends solely on recording density. (See also section 1.9.) 64xx series drives run at 30 inches per second (IPS) and have a data packing density of 6400 bits per inch (bpi). 83xx series drives run at 37.5 IPS, with a density of 8333 bpi. Series xx30 and xx40 drives are specially designed for battery-power applications (see below). Each is capable of high-speed block-search operations.

The direct-drive motor eliminates belts and pulleys and provides tighter control of tape motion. Speed accuracy is enhanced by the use of an optical tachometer. Tape hole markers are detected by a pulsed infrared LED and filtered sensors to reduce the effects of ambient light. For multiple-drive systems, each drive can be configured to respond to one of eight addresses.

Other features include front mounting, very compact size, and an industry-standard interface on the drive that makes it interchangeable with other cartridge units on the market.

The basic functional units of each drive may be described in three groups:

- 1) MECHANISM. The mechanism moves the tape under the control of the two circuit boards. In addition to the capstan motor and tachometer, the mechanism contains the read-after-write head, tape hole sensing assembly, and File Protect and Cartridge-In-Place status switches.
- 2) SERVO BOARD. The Servo Board contains all of the analog electronics. It provides regulated power supplies for the drive, as well as controlling tape motion. It has been computer-optimized to provide high performance at the lowest possible motor power dissipation. The Servo Board also transmits data to the write head, and amplifies and digitizes the signals from the read head. It drives the Tape Hole Detector LED and receives the signals from the Tape Hole Sensors and the File Protect and Cartridge-In-Place switches.
- 3) CONTROL BOARD. The Control Board contains all of the digital electronics. It remembers the tape position, locking out illegal motion commands. It decodes the select lines, latches and clears all commands at the appropriate times, and gates status signals from the drive to the Controller. The Control Board also formats data, converting NRZ write data from the controller to IMFM data for the drive, and IMFM data from the drive to NRZ data and Read Data Strobes for the controller. All signals leaving the board are sent through open-collector drivers and all inputs are to receivers with hysteresis to provide noise immunity.

In addition to the above, xx30 and xx40 series drives are designed for low power usage from +5 and ± 12 volt supplies and to be switched on and off while not reading or writing data. Because of this, there are two major differences in their operation:

- 1) No Automatic Rewind Sequence (ARS) is performed at the time of powering up, since the drive is intended to be powered down during periods of data inactivity (i.e. between data blocks). ARS is performed when remote rewind commands are received and when a tape is inserted into a powered drive.
- 2) Rewind and search speeds are lowered to reduce the power required by the motor. See the specifications chart below.

1.3 SPECIFICATIONS.
(common to
all models)

DRIVE	Single capstan motor drives roller inside cartridge-- no contact between tape and capstan
CAPSTAN SERVO	Velocity feedback from digital tachometer
HEAD TYPE (see Fig. 1.2)	Dual gap read-during-write with selective erase Models xx10 & xx30 - write Forward only Models xx20 & xx40 - write Forward on tracks 1, 3 write Reverse on tracks 2, 4
RECORDING MODE	4 Track serial
RECORDING CODE	Inverted modified frequency modulation Serial by bit
INTERFACE	NRZ (High Density)
PROGRAM TYPE	No Restrictions
DRIVE RELIABILITY	7500 hours Mean Time Between Failures (MTBF)

1.4 SPECIFICATIONS.
(model variable)

	6410/6420	6430/6440	8310/8320	8330/8340
CARTRIDGE TYPE	300', 450' or 555'	Same as 6410/6420	600' only	Same as 8310/8320
RECORDING DENSITY	6400 bpi 252 bits per mm	Same as 6410/6420	8333 bpi 328 bits per mm	Same as 8310/8320
DATA TRANSFER RATE	192,000 bits per sec (6400 bpi @ 30 IPS)	Same as 6410/6420	312,488 bits per sec (8333 bpi @ 37.5 IPS)	Same as 8310/8320
TAPE SPEED, Synchronous	30 IPS (76 cm/s) Fwd/Rev	Same as 6410/6420	37.5 IPS (95.3 cm/s) Fwd/Rev	Same as 8310/8320
TAPE SPEED, Rewind	90 IPS (229 cm/s) ± 5%	60 IPS (152 cm/s) minimum	Same as 6410/6420	Same as 6430/6440
TAPE SPEED, Search (long term, Fwd/Rev)	90 IPS (229 cm/s) ± 5%	60 IPS (152 cm/s) minimum	Same as 6410/6420	Same as 6430/6440
SPEED VARIATION,* Synchronous, Max. (Incl. cartridge effects)	± 3% long term ± 7% short term	Same as 6410/6420	± 3% long term ± 7% short term	Same as 8310/8320
SPEED VARIATION,* Synchronous, Max. (drive only)	± 2% long term ± 3% short term	Same as 6410/6420	± 1% long term ± 3% short term	Same as 8310/8320
CAPSTAN START/STOP TIME at synchronous speed	30 msec ± 5%	Same as 6410/6420	37.5 msec ± 5%	Same as 8310/8320
START/STOP TIMING WAIT DELAY	20 msec Read 40 msec Write, min.	Same as 6410/6420	25 msec Read 45 msec Write, min.	Same as 8310/8320
START/STOP DISTANCE, Synchronous	.375 in. (9.525 mm) ± 10%	Same as 6410/6420	.70 in. (17.86 mm) ± 10%	Same as 8310/8320
START/STOP DISTANCE, Search	3.4 in. (86.3 mm) nominal	Same as 6410/6420	Same as 6410/6420	Same as 6410/6420
INTERRECORD GAP	1.2 in. nominal**	Same as 6410/6420	1.7 in. nominal***	Same as 8310/8320
START/STOP TIME to search speed	90 msec nominal	60-90 msec	Same as 6410/6420	Same as 6430/6440
START/STOP TO SEARCH TIMING WAIT DELAY	100 msec	Same as 6410/6420	Same as 6410/6420	Same as 6410/6420
REWIND TIME	60 sec nominal (450 ft. tape)	90 sec maximum (450 ft. tape)	80 sec nominal (600 ft. tape)	120 sec maximum (600 ft. tape)

NOTES: *Measured per ANSI/ECMA/ISO standards

**During read operations, the drive is capable of reading a minimum Interrecord Gap (IRG) of 1.02 in.

***During read operations, the drive is capable of reading a minimum IRG of 1.4 in.

1.5 VOLTAGE AND CURRENT REQUIREMENTS.

CURRENT REQUIREMENTS IN AMPERES

CONDITION	POSITIVE SUPPLY ¹	NEGATIVE SUPPLY ²	REG. +5V DC SUPPLY ³
STATIC (No Motion)	.13	.07	1.8
REWIND	.73	.07	1.8
FORWARD -- Search	.11	.68	1.8
FORWARD -- Synch.	.11	.53	1.8
REVERSE -- Synch.	.62	.07	1.8
FORWARD RAMP -- Synch.	.32*	1.30**	1.8
REVERSE RAMP -- Synch.	1.30**	.32*	1.8
FORWARD RAMP -- Search	.32*	1.30**	1.8
REVERSE RAMP -- Search	1.30**	.32	1.8

ABSOLUTE MAXIMUM	1.50	1.50	3.0

¹+24V DC Nominal (+18 to +27V DC) for Series xx10 and xx20
+12V DC Nominal (+11 to +14V DC) for Series xx30 and xx40

²-24V DC Nominal (-18 to -27V DC) for Series xx10 and xx20
-12V DC Nominal (-11 to -14V DC) for Series xx30 and xx40

³+4.85 to +5.25V DC -- applies to all models

*Stop Ramp Current

**Start Ramp Current

General Notes:

-All voltages measured at power connector on drive.

-Start/Stop Ramp Currents are pulses with a pulse width of 30 msec to/from 30 ips, 37.5 msec to/from 37.5 ips, and 90 msec to/from 90 ips.

-The ramp period current peaks do not occur simultaneously. A defective cartridge can increase ramp current to the limit of the input fuse or power supply limit.

1.6 ENVIRONMENTAL SPECIFICATIONS.

TEMPERATURE, Operating	+ 5° to +45°C, cartridge limited.
TEMPERATURE, Non-Operating	-30° to +60°C, hardware + 5° to +45°C, cartridge storage -40° to +45°C, cartridge transportation.
HUMIDITY	20% to 80% non-condensing.
ALTITUDE, Operating	10,000 ft (3000 m) maximum.
ALTITUDE, Non-operating	40,000 ft (12000 m) maximum.
VIBRATION, Operating	Tested with 0.5 G, 10 to 60 Hz.
SHOCK, Non-operating	Tested with 50G, 10 ms, half sinewave.
OPERATING ATTITUDE	Any except with the cartridge loaded directly upward; oxide residue from the head may fall into the cartridge and reduce data reliability when mounted in this position.
DUST RESISTANCE	The drive is designed to withstand the dust level of a typical office environment. If used in particularly dusty areas, more frequent cleaning of the head or protecting the equipment with a cover or door is required.
SIZE (max.)	3.5 in (8.9 cm) H x 6.9 in (17.5 cm) W x 5.8 in (14.8 cm) D
WEIGHT (max.)	2.5 lbs (1.13 kg).

1.7 FOUR-TRACK FORMAT

Nominal track width - Read:	.020 inch
Nominal track width - Write:	.036 inch
Nominal track width - Erase:	.048 inch
Nominal track to track spacing:	.064 inch
Nominal write to read gap spacing:	.300 inch
Nominal write to erase gap spacing:	.265 inch (xx10 & xx30)
Nominal write to erase gap spacing:	.225 inch (xx20 & xx40)

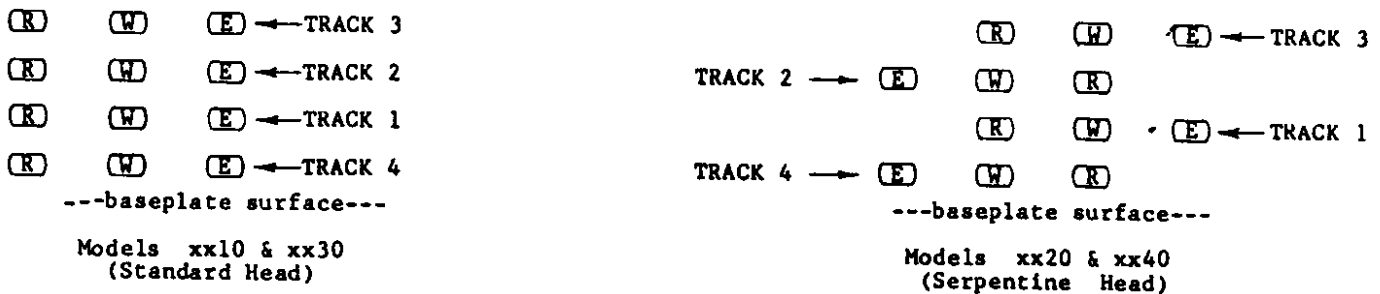


Figure 1.2, Head Configuration (Front View). Arrows indicate direction of tape motion for active data transfer.

1.8 ERROR RATES. The error rates listed below are design goals measured at the cartridge drive interface before the formatter or controller performs any error correction. For these measurements, the minimum allowable record consists of 18 data bits. Cartridges must meet ANSI X3.55 specifications while operating in temperatures from 5°C to 45°C with a relative humidity of 20% to 80% and must be full-length certified at full recording density. Errors caused by tape with damaged oxide shall not be included in the error rate unless the damage is caused by the drive during test.

1.8.1 DEFINITIONS.

- 1) Recoverable Errors - Those existing for less than five retries of writing or reading.
- 2) Permanent Errors - Those persisting after five reread or rewrite attempts (including an extended erased gap with each rewrite). These errors constitute an equipment failure and are included in the MTBF.

1.8.2 WRITE ERROR RATE. The recoverable write error rate will not exceed one error in 10^7 bits. The permanent write error rate will not exceed one error in 10^9 bits.

1.8.3 READ ERROR RATE. When reading a tape with no write errors, the recoverable read error rate will not exceed one error in 10^7 bits. The permanent read error rate will not exceed one error in 10^9 bits.

1.9 CARTRIDGE COMPATIBILITY. Due to differences in the magnetic properties of the tapes, it is recommended that only 300-foot, 450-foot, or 555-foot cartridges be used on low density (64xx series) drives and only 600-foot High Density cartridges be used on high density (83xx series) drives.

2) INSTALLATION

2.1 INTRODUCTION. This chapter describes the installation procedures for the drive. (NOTE: Interfacing is described in detail in Chapter 3.)

2.2 INSTALLATION PROCEDURE. Digi-Data Cartridge Drives come completely calibrated and ready to install in a system. No test equipment or technical training is needed. Installation requires only a few simple steps:

- 1) Plug the cable from the controller onto the interface connector at the rear of the drive, on the Control (lowest) Board. See figure 3.3. Pin number one is indicated by a number on the board. The drive requires a 50-pin connector (3M #3425-7000 or equivalent).
- 2) Plug the power cable onto the connector on the right side of the Servo (inner) Board. The plug should be keyed so that it can be attached only one way. See section 3.2.3.
- 3) If the drive is to be installed as one unit per controller, skip to paragraph (4).

The Digi-Data Cartridge Drive is designed so that up to eight units may be daisy-chained (connected in parallel) to one controller. In this type of system, each tape unit must be assigned a number so that the controller can select each individually. As shipped, each drive is configured to be selected as Unit 0. Therefore, in a multiple-drive system, all units after the first must be re-configured to a different select number. This can be done as follows:

- A. Turn the drive upside-down, with its front toward you. You will see the Control Board (labeled "82CDC"). At the extreme right side of the board you will find either three 10-ohm resistors, or a DIP switch, labeled "RSL 4 1 2".

RESISTORS: Removing a resistor adds its assigned number to the tape unit select number. For example:

Tape Unit as shipped	=	Unit # 0
Remove RSL 1	=	Unit # 1 (0 + 1)
Remove RSL 1 & 4	=	Unit # 5 (0 + 1 + 4)

Determine the Unit Select Number to be assigned to the drive. Using a small pair of wire cutters, clip each resistor close to the board on each end and remove from the board.

SWITCH: Unit Number selection is analogous to the resistor method described above, except that you set the designated switches off instead of removing resistors.

In summary,

To Set This Tape Unit Number	Remove These Resistors	OR	Turn These Switches OFF
0	DO NOTHING !		ALL ON
1	RSL 1		RSL 1
2	RSL 2		RSL 2
3	RSL 2 + RSL 1		RSL 2 + RSL 1
4	RSL 4		RSL 4
5	RSL 4 + RSL 1		RSL 4 + RSL 1
6	RSL 4 + RSL 2		RSL 4 + RSL 2
7	RSL 4 + RSL 2 + RSL 1		RSL 4 + RSL 2 + RSL 1

- B. For all drives except the LAST in the chain you will also need to change the terminator pack on the Control Board. The Pack is in the socket at location U9B. As shipped, each drive contains a 220/330 terminator (i.e. 220 ohms to +5V and 330 ohms to GND). For all intermediate drives in the chain, lift the pack out of the socket and replace it with a 4.7k-ohm resistor pack (i.e. 4700 ohms to +5V). See section 3.2 for more details.

4) Attach the drive to the housing with four 8-32 screws of the appropriate length (panel thickness + 1/4 inch maximum).

3) INTERFACE AND CONTROL

This chapter describes the electrical and physical interface requirements and defines all interface signals.

3.1 ELECTRICAL INTERFACE REQUIREMENTS. The cartridge drive and its controller exchange all information (commands, status, and data) through the drive's interface. All signals are TTL (low true) and pass through dedicated interface lines. For all output signals, line drivers are 7406 open-collector buffers or the equivalent, capable of sinking 40 mA; receivers are 7414 thres-holded devices or the equivalent. As shipped, all inputs are terminated in a 220/330 terminator pack (i.e. a 220 Ohm resistor to +5V and a 330 Ohm resistor to ground) to keep the signals from the controller at proper TTL high or low levels. This is correct for solitary drives, but when the system requires that more than one drive be daisy-chained (connected in parallel) to one controller, the terminator on all drives EXCEPT the LAST in the chain must be changed to a 4.7k ohm resistor pack. For convenience, the terminator is socket-mounted at location U9B on the Control Board. See Figure 3.1.

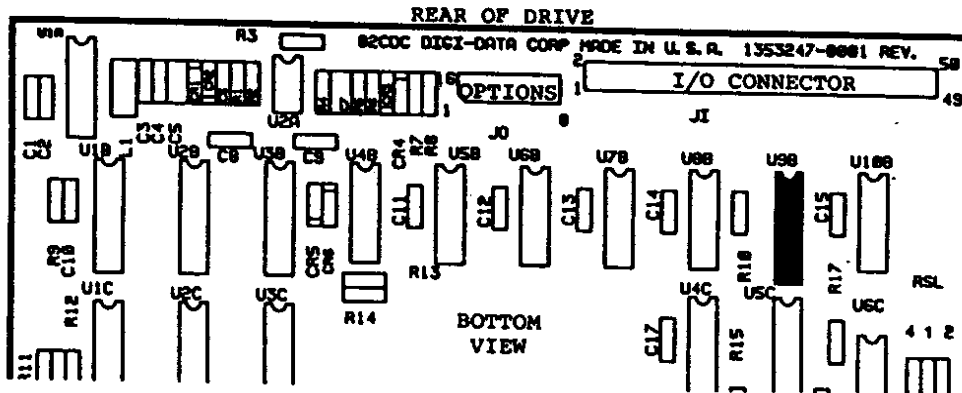


Figure 3.1, Bottom Rear of Drive

The controller should drive all inputs using open-collector circuits capable of sinking at least 30 milliamps while maintaining the logic levels listed below. The recommended interface circuit is shown in figure 3.2.

Logic True Level = LOW = 0 to 0.4 VDC
 Logic False Level = HIGH = 2.5 to 5 VDC

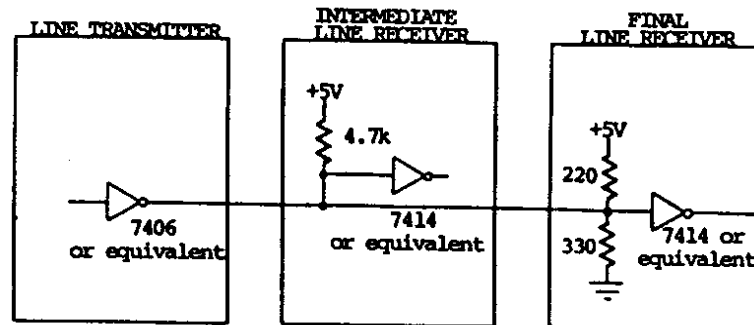


Figure 3.2, Recommended Interface

The minimum recommended pulse width on the interface line (except for DAD±) is 500 nanoseconds. Inputs which elicit immediate confirming responses from the drive may be narrower if they go false upon detecting the drive's response. Rise and fall times should not exceed 100 nsec.

3.2 PHYSICAL INTERFACE REQUIREMENTS.

3.2.1 CONTROLLER I/O. The 50 pin male interface plug on the drive is located at the right rear of the Control Board. It mates with 3M Company connector part no. 3425-7000 and cable part no. 3350 50-conductor or equivalents.

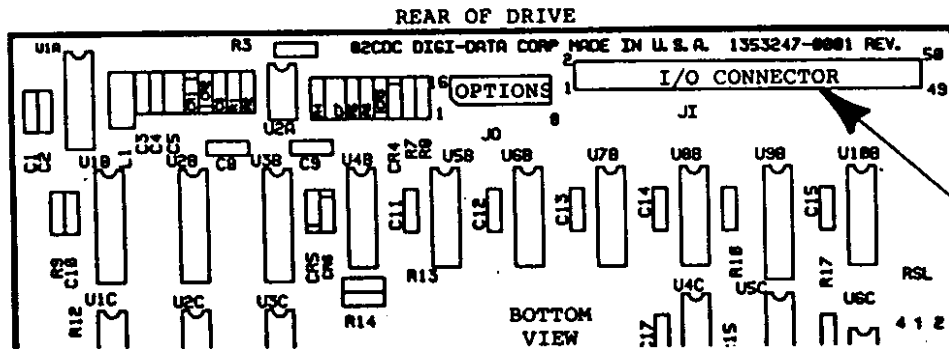


Figure 3.3, Controller I/O

3.2.2 OPTIONS CONNECTOR INTERFACE. The 16 pin female interface DIP socket at the rear center of the Control Board mates with standard male DIP connectors.

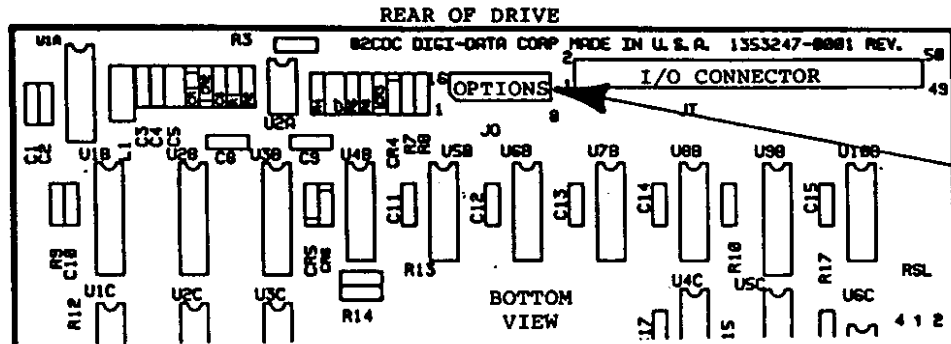


Figure 3.4, Options Connector

3.2.3 DRIVE POWER CONNECTOR INTERFACE. The 16 pin male connector on the Servo Board mates with the following AMP Corporation parts or their equivalents:

- Connector - AMP Part No. 1-86148-5 (1 ea)
- Contact Pins - AMP Part No. 86016-4 (13 ea)
- Keying Plugs - AMP Part No. 86286-1 (3 ea)

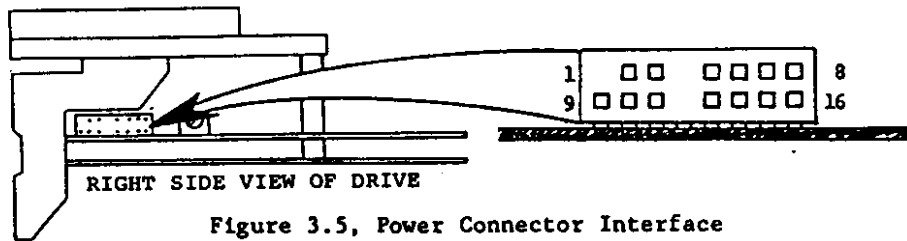


Figure 3.5, Power Connector Interface

3.2.3.1 WIRING.

A. Chassis Ground is the physical case of the drive. Servo common returns the unregulated supplies' currents. Logic common returns the +5 VDC current. All three are separate within the drive. All three must be tied together and to ground at a single point within the power supply.

B. Hookup wire size = #22 AWG.

C. See Section 1.5 for power requirements.

3.2.3.2 FUSING. The positive, negative, and +5 VDC power supply lines to the drive should have a Bussman AGC 3A, 250V Fast-Blo (or equivalent) fuse in series with them.

3.4 SIGNAL DESCRIPTIONS. (Note: All are TTL Low True.)

SIGNAL	NAME	DESCRIPTION
BSY-	BUSY	<p>BUSY, gated by RDY, indicates that the drive is presently moving tape. BUSY goes true when the tape begins moving and remains true approximately 30 msec after the motion command is cleared (37.5 msec in 83xx series drives, and 95 msec during high speed operations) to allow time for the tape to ramp down completely.</p> <p>BUSY will not go true if a REVERSE command is received when the tape is at BOT or if a FORWARD command is received when the tape is at EOT.</p>
DAD-	DATA DETECTED	<p>DATA DETECTED indicates that valid read data is being received with no interruptions in the data flow. It comes true 20 usec after the beginning of the preamble (in low speed operation) to permit the Control Board to verify that a proper preamble has been received. The signal then remains true for the duration of the data block or until a large (40 usec nom.) dropout occurs. When reading, DAD should be monitored continuously since it may go false momentarily during the middle of a record if a dropout occurs. The controller must therefore take care when backspacing over an error record for rewriting so that it does not interpret the momentary dropout in DAD as an interrecord gap or else the rewrite operation will begin at an incorrect place on tape. During high speed searches, DAD can be monitored to detect data blocks.</p>
EWS-	EARLY WARNING SENSED	<p>EARLY WARNING, gated by RDY and not rewinding, indicates that the Early Warning tape hole has been passed while moving forward. Between this tape hole and the EOT marker there are 48 inches of tape, 36 inches of which are useable for data recording. EWS remains true until the Early Warning tape hole is passed while moving reverse. The Control Board prevents high speed tape motion (except rewinding) when EARLY WARNING is true.</p> <p>Note that in Low Power models (xx30 and xx40), this signal is false upon power up even if the drive is positioned at or beyond the Early Warning tape hole. At power up, these models do not remember their status nor perform an Auto Rewind Sequence but assume that the tape is positioned between the Load Point and Early Warning markers. It is up to the controller to keep track of the status of these drives; if not, it would be possible to run the tape beyond EOT.</p>
FLG-	FLAG	<p>FLAG, gated by RDY, indicates that a rewind sequence has been completed, the tape is positioned between the two BOT markers farthest from the take-up hub, and the drive has ramped down. FLAG remains true until the drive executes a forward operation. This signal is false upon power up in Low Power Models (xx30 and xx40), since the drive does not rewind on power up.</p>
FUP-	FILE UNPROTECTED	<p>FUP, gated by RDY, indicates that the cartridge presently installed can be written on. When false, FUP indicates that the cartridge's file protect switch is in the "SAFE" position.</p>
FWD-	FORWARD	<p>FORWARD commands the drive to move tape forward at the speed specified by HSP. The drive will execute the command if RDY is true, the drive is not already moving tape, and it is not at EOT. Acceleration and deceleration rates are constant; ramp up and ramp down times are nominally equal. When FORWARD is cleared the servo brakes the motor and the drive ramps down. Another FWD command given during the ramp down time will be executed immediately; a REV command will be executed as soon as the tape stops moving. If FWD is set at the same time as REV, the drive will ramp to a halt and remain halted until one of the commands is cleared.</p>

3.3 SIGNAL LOCATIONS.

3.3.1 CONTROLLER I/O.

<u>DRIVE OUTPUTS</u>			<u>DRIVE INPUTS</u>		
<u>PIN NO.</u>	<u>SIGNAL</u>	<u>NAME</u>	<u>PIN NO.</u>	<u>SIGNAL</u>	<u>NAME</u>
2	SLD-	Selected-	18	RWD-	Rewind-
4	RDY-	Ready-	20	REV-	Reverse-
6	WND-	Write Enabled-	22	FWD-	Forward-
8	FLG-	Flag-	24	HSP-	High Speed
10	LPS-	Load Point Sensed-	26	WEN-	Write Enable-
12	FUP-	File Unprotected	28	SL1-	Unit Select 2 ⁰ -
14	BSY-	Busy-	30	SL2-	Unit Select 2 ¹ -
16	EWS-	Early Warning Sensed-	32	SL4-	Unit Select 2 ² -
36	RNZ-	Read NRZ Data-	34	SLG-	Select Gate
38	RDS-	Read Data Strobe-	42	WDE-	Write Data Enable-
40	DAD-	Data Detected-	44	WNZ-	Write NRZ Data-
48	WDS-	Write Data Strobe-	46	TR2-	Track Select 2 ¹
			50	TR1-	Track Select 2 ⁰

NOTE: All odd-numbered pins are ground returns for the signals on the following even-numbered pins and are tied together.

3.3.2 OPTIONS CONNECTOR.

<u>PIN NO.</u>	<u>SIGNAL</u>	<u>TYPE</u>	<u>SIGNAL NAME</u>
1	SL-I	OUTPUT	Selected - Inverted
5	RWD-I	INPUT	Rewind - Inverted
6	FIPD-I	OUTPUT	File Protected - Inverted
7	BOTD-I	OUTPUT	Beginning of Tape - Inverted
8	BSYD-I	OUTPUT	Drive Busy - Inverted
9	+5	OUTPUT	+5 Volts
11	GND		Ground

NOTE: Pins 2, 3, 4, 10, 12, 13, 14, 15, 16 are all unused (No Connection).

3.3.3 DRIVE POWER CONNECTOR.

<u>PIN NO.</u>	<u>SIGNAL</u>	<u>SIGNAL NAME</u>
1	N/C--Key Pin	No Connection (cut off)
2,10	+ VDC	Positive power supply (24V or 12V)
3,11	- VDC	Negative power supply (24V or 12V)
4,12	N/C--Key Pin	No Connection (cut off)
5,13	SC	Servo common from power supply
6,14	+5 VDC	Regulated +5 VDC from power supply
7,15	LC	Logic common from power supply
8,16	CG	Chassis ground from drive
9	N/C	no connection

xx30 and xx40 drives do not remember their position upon power up, so it may be possible to run these forward past EOT. See the description of Early Warning, above.

HSP- HIGH SPEED HIGH SPEED commands the servo to move tape at search speed in the direction selected by FWD or REV. High speed motion can only be executed between the Load Point hole (LP) and the Early Warning hole (EW); outside this region the HSP line is ignored. It is not necessary to set HSP to rewind.

Note that xx30 and xx40 drives upon power up do not remember where the tape is positioned. Therefore, it is up to the controller to take care not to issue HSP outside the legal zone.

LPS- LOAD POINT SENSED LOAD POINT, gated by RDY and not rewinding, indicates that the Load Point tape hole has been passed while moving reverse. LPS remains true until the Load Point tape hole is passed while moving forward. The Control Board prevents high speed tape motion (except rewinding) when LOAD POINT is true.

Note that in Low Power models (xx30 and xx40), this signal is false upon power up even if the tape is positioned at or before the Load Point tape hole. At power up, these models do not remember their status nor perform an Auto Rewind Sequence but assume that the tape is positioned between the Load Point and Early Warning markers. It is up to the controller to keep track of the status of these drives; if not, it would be possible to run the tape before BOT.

RDS- READ DATA STROBE The READ DATA STROBE indicates to the controller that the RNZ lines are stable and can be sampled. It occurs once per character period and has a 25% duty cycle. (At 6400 bpi, the character period is 5.2 ±.52 usec; 25% duty cycle is 1.3 ±.13 usec. At 8333 bpi character period is 3.2 ±.32 usec, duty cycle is 800 ±80 nsec.) RNZ will be stable 200 nsec before RDS and will remain stable for the duration of the strobe. The data may be changed on the trailing edge of RDS or at any time thereafter, but will be stable 200 nsec before the next read strobe.

RDY- READY READY indicates that the drive is powered up, has a cartridge in place, and is selected.

REV- REVERSE REVERSE commands the servo to move tape in the reverse direction at the speed specified by HSP. The drive will execute the command if RDY is true, the drive is not already moving tape, and it is not at BOT. Acceleration and deceleration rates are constant; ramp up and ramp down times are nominally equal. When REVERSE is cleared the servo brakes the motor and the drive ramps down. Another REV command given during ramp down time will be executed immediately; a FWD command will be executed as soon as the tape stops moving. If FWD and REV are set at the same time the drive will ramp to a halt and remain halted until one of the commands is cleared.

xx30 and xx40 drives do not remember their position upon power up, so it may be possible to run these reverse past BOT. See the description of Load Point Sensed, above.

RNZ- READ NRZ DATA READ NRZ DATA is the NRZ read data to the controller. A zero is indicated as a high and a one as a low. RNZ will be stable at least 200 nanoseconds before RDS and will remain stable for the duration of the strobe.

RWD- REWIND REWIND initiates an Automatic Rewind Sequence to BOT. If RDY is true, the command is accepted. All subsequent commands are ignored until the operation is complete. The drive may be deselected during the rewind sequence without affecting the operation.

The rewind sequence begins by moving tape forward at high speed for approximately .6 seconds to be sure the first three BOT markers are cleared. The tape then ramps down and begins moving reverse at high speed until a BOT marker (the one farthest from the hub) is sensed. The Done Flag (FLG) signals a completed Rewind after the tape ramps to a halt.

SL1- SELECT2⁰
 SL2- SELECT2¹
 SL4- SELECT2²

The select lines select one of up to eight drives (daisy-chained) on the interface. If a drive is addressed it will respond to motion commands and place its status on the bus. Two drives should not be configured to respond to the same address or both drives will place their status on the bus simultaneously.

The drive select number is decoded as the sum of whichever Select Lines are true (low). See the chart below. When the drive is shipped, it is configured to respond as Unit 0 (all SL- lines high). To configure the drive to a different address, remove the RSL resistor(s) or set the switches corresponding to the SL- line(s) that are low for that address. See the chart below and Section 2.2.2.

TAPE DRIVE SELECTED	SL4-	SL2-	SL1-
0	H	H	H
1	H	H	L
2	H	L	H
3	H	L	L
4	L	H	H
5	L	H	L
6	L	L	H
7	L	L	L

SLD- SELECTED SELECTED indicates that a drive has responded to the address select lines.

SLG- SELECT GATE SELECT GATE is sent by the controller to indicate whether the address on the SELECT lines is valid. The controller must maintain proper SELECT GATE status at all times. SELECT GATE should be cleared before the select lines are changed.

TR1- TRACK1 The TRACK lines are decoded to select the data track to be accessed.

TR2- TRACK2

ANSI TRACK NUMBER	TR2-	TR1-
1	H	L
2	L	H
3	L	L
4	H	H

The controller must maintain proper track selection during all operations. When a drive is deselected, the TRACK lines are latched to avoid the wait for stabilization when reselected. Track selection should not be changed while the drive is write enabled or within two milliseconds after WND is cleared to prevent damaging data on other tracks. The TRACK lines should be set before asserting WEN or ERA.

WDE- WRITE DATA ENABLE WRITE DATA ENABLE allows the drive to begin encoding WNZ into IMFM write data. WDE must be set within 5.2 microseconds (3.2 usec for 83xx drives) before the first bit of the preamble and must remain true for the entire data record, including preamble and postamble.

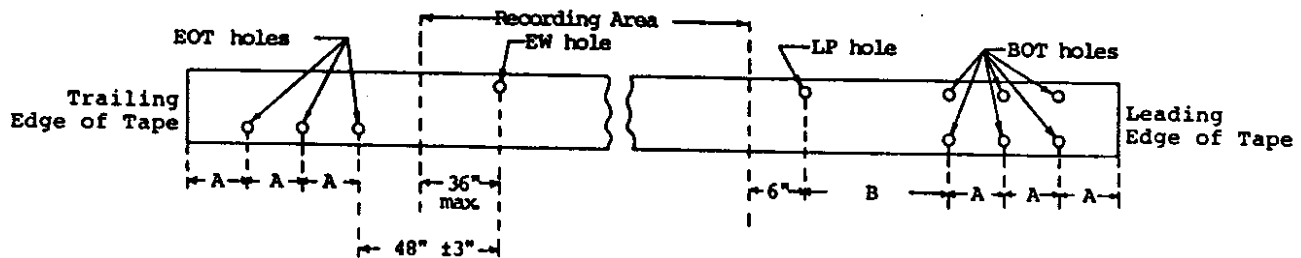
WDS- WRITE DATA STROBE The WRITE DATA STROBE is a 25% duty cycle pulse occurring every character period. It indicates that the drive is sampling WNZ. WNZ may be changed at any time after the trailing edge of WDS, but it must be stable within 3.7 microseconds (2.2 usec for 83xx drives) to be ready 200 nanoseconds before the next WDS.

4) TAPE AND DATA FORMATS

4.1 INTRODUCTION. This chapter describes the ANSI Standard for data cartridges (ANSI X3.55-1977) and the IMFM data format.

4.2 TAPE FORMAT. The tape format is illustrated in figure 4.1. Tape regions are marked by small holes in the tape. These holes are sensed by a pulsed infrared LED and two detectors on the drive. The drive uses the direction of tape motion and the tape hole signals to determine the tape's position and which motion commands are legal.

Beginning of Tape (BOT) is marked by three sets of simultaneous upper and lower holes, beginning 18 inches from the physical beginning of tape and spaced 18 inches apart. Beyond the last set is Load Point (LP), a single upper tape hole. Then follows the main recording area of the tape. Another single upper tape hole signals Early Warning (EW), 48 inches before End of Tape (EOT). The drive's logic distinguishes between the LP and EW by the direction of tape travel and by the last marker hole seen. EOT is marked by three single lower tape holes spaced 18 inches apart, the last of which is 18 inches from the physical end of the tape. BOT and EOT are redundantly marked by three sets of holes each to help ensure that the tape will not be run off the reels.



A = 18" ± 3"
 B = 36" ± 3" except on newer 600A cartridges where B = 48"

Figure 4.1, Tape Format

Starting from BOT, standard drives begin recording data after the LP hole has been passed while going forward and continue until after the EW marker hole. EW serves to signal the controller that data activity must cease soon; all forward motion ends when EOT is reached. Between LP and EW all High and Low Speed and Forward and Reverse operations are allowed; no high speed (except rewind) is permitted beyond EW or before LP to protect the tape. When moving reverse, all motion stops at BOT. Serpentine drives perform the same on tracks 1 and 3, but on tracks 2 and 4 writing and reading is in reverse, so the tape regions are treated oppositely--Starting at EOT, there is no recording before EW, and LP serves to warn that BOT will soon be reached and the tape will stop.

TAPE	TAPE ZONE	LEGAL COMMANDS (Standard Drives)	LEGAL COMMANDS (Serpentine Drives)
	BOT ZONE	Low Speed Forward - No Data Transfer	Low Speed Forward - No Data Transfer Tracks 1 & 3
• •	BOT	Low Speed forward and Reverse - No Data Transfer	Read Forward Tracks 2 & 4 Low Speed Forward and Reverse - No Data Transfer Tracks 1 & 3
	LPS	Rewind	Read Rev and Fwd Tracks 2 & 4 Write Reverse Tracks 2 & 4
•	LP Hole	High/Low Speed Fwd and Rev	Rewind
	Recording Area	Read Forward/Reverse Write Forward Rewind	High/Low Speed Fwd and Rev Read Forward and Reverse Write Forward Tracks 1 & 3 Write Reverse Tracks 2 & 4
•	EW Hole	Low Speed Forward and Reverse Read Forward and Reverse	Rewind
	EWS	Write Forward Rewind	Low Speed Forward and Reverse - No Data Transfer Tracks 2 & 4 Read Fwd and Rev Tracks 1 & 3 Write Forward Tracks 1 & 3
•	EOT	Low Speed Reverse	Rewind
	EOT ZONE	Read Reverse Rewind	Low Speed Reverse - No Data Transfer Tracks 2 & 4 Read Reverse Tracks 1 & 3 Rewind

Figure 4.2, Legal Tape Commands

4.3 IMFM DATA FORMAT. IMFM is a self-clocking data code. Each Digi-Data Cartridge Drive contains its own IMFM formatting circuitry as part of the Control Board, and is ready to receive data records encoded in NRZ from the controller. A record consists of three parts: preamble, data, and postamble.

Data coding is context sensitive. A zero preceded by a zero is encoded as a magnetic flux transition at the beginning of the bit cell; a zero not preceded by a zero (i.e. at the beginning of the preamble or following a one) does not have a transition associated with it. Ones are always represented as a flux reversal in the center of the bit cell. See figure 4-3 below for sample data and waveforms.

Since transitions may occur both at the beginning and in the middle of a bit cell, the decoding circuits must be synchronized with the data before attempting to read. A preamble therefore precedes the data to provide a standard pattern that the formatter decodes to establish proper timing. Generally, the preamble consists of at least 39 zeros followed by a single one; there is no standard, however, and there is some variation in preamble formats. Digi-Data's IMFM Formatting circuitry synchronizes on a minimum of 39 zeros followed by a one to make it compatible with most of the controllers on the market. The controller must send the preamble encoded in NRZ; the Control Board then converts it to IMFM. When reading a preamble, the Control Board synchronizes on the all zeros portion and, after encountering the one at the end of the preamble, transmits the NRZ data and strobe derived from the IMFM data. A postamble follows the data to allow synchronization when reading reverse.

There is no standard for file marks; each controller must generate and decode them based on the manufacturer's specifications. It is recommended that the file mark be at least 100 bits long to allow for proper detection in high speed search mode. The controller is also responsible for generating the appropriate gaps after file marks and at the end of records.

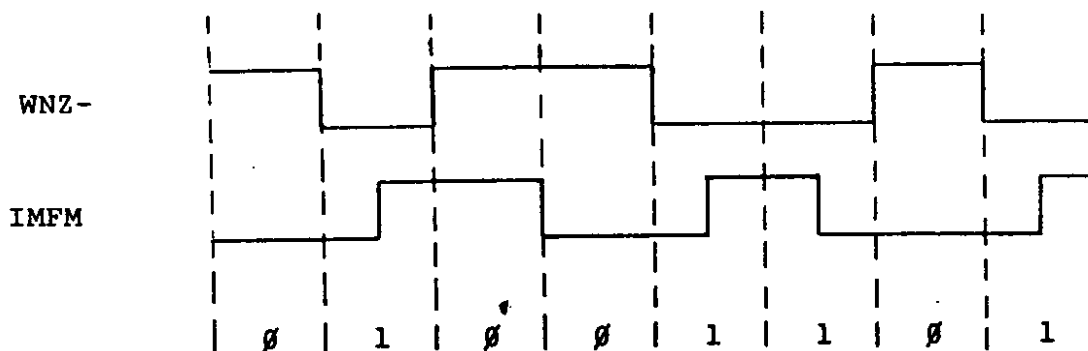


Figure 4-3, Sample Data Waveforms

5) TAPE OPERATIONS

5.1 INTRODUCTION. This chapter describes drive and track selection, data transfer operations, High Speed Searches, and rewinds. It begins with a brief summary of each operation and then explains the controller timing at the interface.

5.2 SUMMARIES OF OPERATIONS.

5.2.1 PREPARING THE DRIVE. Before any tape operation can be executed the controller must select the drive, receive the appropriate status signals and set the track lines.

The controller can individually select each drive connected to it by addressing the unit select lines. Each drive can be configured to respond to a different unit select number (0 - 7). See the chapter on installation, section 2.2 (2).

Before any operation can begin the drive must be selected, and a cartridge must be inserted. This is indicated by the output signal RDY (Ready).

Once a drive is selected and has a cartridge inserted, the track lines should be set. (During rewind track selection is irrelevant.) These lines specify the track to or from which data is to be transferred. The lines must be set before any data transfer or search operation begins and must remain stable throughout the operation. During read operations the track lines should not be changed until the tape halts (BUSY goes false). When changing from write to read, the controller should wait at least 2 milliseconds after WND goes false before changing track selection.

5.2.2 WRITE OPERATIONS. Write Operations receive data from the controller and record it on tape. The drive will receive NRZ data with a Write Data Strobe and convert it to IMFM. The data is recorded serially on one of four tracks. Write Operations can only be executed in low speed forward on Standard models; on Serpentine models, writing is forward on tracks 1 and 3, and in reverse on tracks 2 and 4.

To prevent accidental erasure, several internal status signals are required before the Write Operation can be performed. The SAFE switch on the cartridge must be in the unprotected position; this will be indicated by FUP- true. RDY must be true and the track lines must be set. After the track lines are stable Write Enable (WEN) must be set.

Once WEN is set the Write Operation may begin by asserting FWD (Forward). After the drive ramps up to speed (the prerecord delay), the preamble (supplied by the controller) is written on tape. The data follows, ending with the controller-generated postamble.

After the postamble has been written, the controller should wait until the entire postamble has passed the read head to complete the read after write check. After an extended postrecord delay (at least 2.5 msec longer than the read delay) the motion command may be removed. When the tape has halted (BUSY goes false), WEN may be removed. A new track may not be selected until at least 2 msec after WND is cleared; WND is cleared when a motion command is received that would be illegal for writing. That is High Speed (HSP), Rewind (RWD), Reverse (REV) on standard drives; and on serpentine drives, Reverse on tracks 1 and 3, Forward (FWD) on tracks 2 and 4.

5.2.3 READ OPERATIONS. Read Operations transfer data from tape to the controller. The MFM Formatting circuitry converts the MFM data into NRZ data and Read Data Strokes and strips off the preamble. The drive can read bidirectionally, subject to controller limitations. No high speed read operations may be performed, however.

To initiate a Read Operation, RDY must first be true. The track lines should then be set, followed by the Forward or Reverse motion command. As long as HSP and WEN are not asserted, a read operation will take place. The track lines must be stable or the data will be unreliable. The Read Data is transmitted over the RNZ line. Data Detected (DAD) will be true when the RNZ line is valid and can thus be sampled. The RNZ line should only be sampled while DAD is true. NOTE: During the first 20 msec of the acceleration ramp it is recommended that RNZ not be sampled regardless of the status of DAD. The drive will begin transferring data to the controller immediately following the "one" in the preamble.

To end a Read Operation, the controller should first wait until the last data word is transferred and the postamble is completed. At that point DAD will go false. After a short postrecord delay (less than 100 usec) the controller should either remove the motion command or begin another operation "on-the-fly." Once the tape halts completely (BUSY goes false) the track lines may be changed safely.

5.2.4 HIGH SPEED SEARCH OPERATIONS. The High Speed Search Operation moves tape either Forward or Reverse under controller direction. Generally, the controller monitors DAD and counts how many records pass the read head to determine when to end the operation.

The sequence of commands for a High Speed Search Operation is very similar to a Read Operation, except that HSP is asserted before the motion command. The drive must be selected and RDY must be true; the track must be selected; HSP must then be set; lastly, the motion command must be asserted. When the drive has spaced the appropriate number of records, it should be decelerated and stopped. During deceleration, however, the drive will probably overshoot into the following data blocks; the drive must then return to the correct block. There are many ways to do this, depending on system formats and requirements. One common method is given below.

After spacing the appropriate number of records, remove HSP. Continue counting DADs while the tape ramps to synchronous speed. Once the drive is moving at synchronous speed, decelerate it to a halt at the end of the next data block. It should come to a stop between records. To return to the correct place on tape, space reverse in low speed (to prevent the tape from overshooting the gap again) the number of records passed during the ramp down. Once the tape halts (once again in the gap) the desired data can be read.

5.2.5 REWIND OPERATIONS. The Automatic Rewind Sequence begins with .6 seconds of high speed forward motion (to guarantee clearance of all three BOT markers), followed immediately by high speed reverse to the first BOT marker encountered (i.e. the one farthest from physical beginning of the tape). Once a BOT marker is encountered, the tape ramps down immediately. This is the only operation that can be performed while the track lines are changing.

There are several ways to initiate a rewind sequence. The controller can command a rewind operation by setting RWD low. A Rewind may be initiated manually through the RWD input to the Option Connector. A rewind sequence is also executed whenever a cartridge is inserted if the drive is powered up. With Models xx10 and xx20 only, if a cartridge is in place but the drive is not powered up, a rewind will occur when power does come on.

5.3 CONTROLLER TIMING DIAGRAMS. The timing requirements for the major tape operations on each model of the drive are illustrated in the following timing diagrams with comments accompanying them. Note the following conventions:

- (1) The timing diagrams are drawn from the controller's perspective rather than from the perspective of a specific drive: the status signals shown are for the selected drive. While no drive is selected (e.g. while drive selection is changing) the status signals are not valid.
- (2) Whenever a signal is invalid (and therefore not to be examined) it is shaded in.
- (3) All boxed signal names on the timing diagrams represent controller inputs from the drive, and all unboxed signals are controller outputs.
- (4) All signals are TTL low true.
- (5) There is no rigid time scale in the drawings; all significant times are labeled. Where dual times are given, the first figure is for 64xx drives, the figure in () is for 83xx drives.

5.3.1 WRITE OPERATIONS. The timing diagram (figure 5.1) for the write operation also includes drive deselection and reselection. Note the following:

- (1) The track lines must be completely stable before SLG comes true. While the drive is selected, the track lines may only be changed if the drive has not been Write Enabled (WND) for at least 2 milliseconds and if the tape is not moving.
- (2) While drive selection is changing the status signals should be ignored.
- (3) WEN is a 300 nanosecond pulse (minimum). The leading edge of WEN sets and latches WND (Write Enabled). The drive remains write enabled until either a high speed or an illegal-for-write motion command is executed. Thus, even though the drive is deselected and then reselected, WND remains latched. Note that when Drive 2 is reselected the track lines must return to TRK 2 because WND is still latched. Track selection may be changed two milliseconds after WND is cleared if the tape is not moving.
- (4) The prerecord delay (delay from FWD to WDA) should be at least 40 milliseconds.
- (5) DAD should be ignored until the write data transmission begins (at least 40 milliseconds after the FWD motion command). As soon as FWD goes false DAD again should be ignored.
- (6) After DAD goes false there is a 2.5 millisecond (minimum) post-record delay before FWD is removed.

Write operations performed from BOT (figure 5.2) are identical to normal write operations except that the prerecord delay must extend at least 200 milliseconds after LPS goes false.

5.3.2 READ OPERATIONS. The read operation is shown in figure 5.3. Note the following:

- (1) While drive selection is changing the status signals should be ignored.
- (2) DAD should be ignored for at least 20 milliseconds after FWD is asserted. It should be ignored again as soon as FWD goes false.
- (3) The post-record delay is very short for read operations. The write delay is 2.5 milliseconds (minimum) to produce a sufficiently long interrecord gap; the read delay is very short to ensure that the gap written onto the tape is long enough to allow for deceleration and acceleration into the next record without encountering data.

Read operations performed from BOT are identical to normal read operations except that DAD should be ignored for at least 100 milliseconds after LPS goes false.

5.3.3 HIGH SPEED SEARCH OPERATIONS. Figure 5.4 shows a high speed search following a write operation (WND true). Items to note are:

- (1) The motion command may be either FWD or REV, with the other held false through the entire operation.
- (2) The track lines must be stable for the duration of the operation.
- (3) WND goes false as soon as the motion command is asserted (with HSP true).
- (4) DAD should be ignored for the first 20 milliseconds after the motion command. The controller may count DADs during the deceleration to enable the drive to place the tape in the correct interrecord gap (not shown).

5.3.4 AUTOMATIC REWIND SEQUENCE. The Automatic Rewind Sequence (see figure 5.5) is shown beginning past the EW tape hole following a write operation (WND true). Items to note are:

- (1) WND goes false as soon as RWD comes true.
- (2) RWD is a 300 nanosecond (minimum) pulse. Although the tape moves at high speed, HSP should not be set.
- (3) EWS and LPS are both suppressed during the rewind until BOT is reached.
- (4) The Select lines must be stable. The track lines should be changed only after BOT is reached.

5.4 DATA SIGNALS. The following paragraphs discuss timing for the write and read data signals.

5.4.1 WRITE DATA. The write data is input to the drive as NRZ. The relevant signals are shown in figure 5.6. Note the following:

- (1) The preamble, data, and postamble must be presented already encoded in NRZ.
- (2) The first zero of the preamble should be on WNZ 200 nanoseconds before WDE. WDE should be cleared on the positive going edge of the last WDS in the postamble.
- (3) WDS is a 25% duty cycle pulse that occurs once per bit. Data is clocked in on the negative going edge of the strobe.
- (4) Each bit must be stable on WNZ at least 200 nanoseconds before the clock. It may be changed on or after the positive going edge of WDS but must again be stable 200 nanoseconds before the next clock.

5.4.2 READ DATA. The read data is an output to the controller from the IMFM Formatter. The relevant signals are shown in figure 5.7. Note the following:

- (1) The IMFM Formatting circuitry is designed to strip the preamble from the data transmitted to the controller. It will always transmit the postamble and a few "garbage" cells after the postamble until DAD goes false.
- (2) DAD will come true within the first seven zeros of the preamble. DAD will go false after the end of the postamble.
- (3) RDS is a 25% duty cycle pulse that occurs once per bit. Data is clocked in on the negative going edge of RDS.
- (4) Each bit will be stable on RNZ at least 200 nanoseconds before the clock. It may be changed on or after the positive going edge of RDS but will again be stable 200 nanoseconds before the next clock.

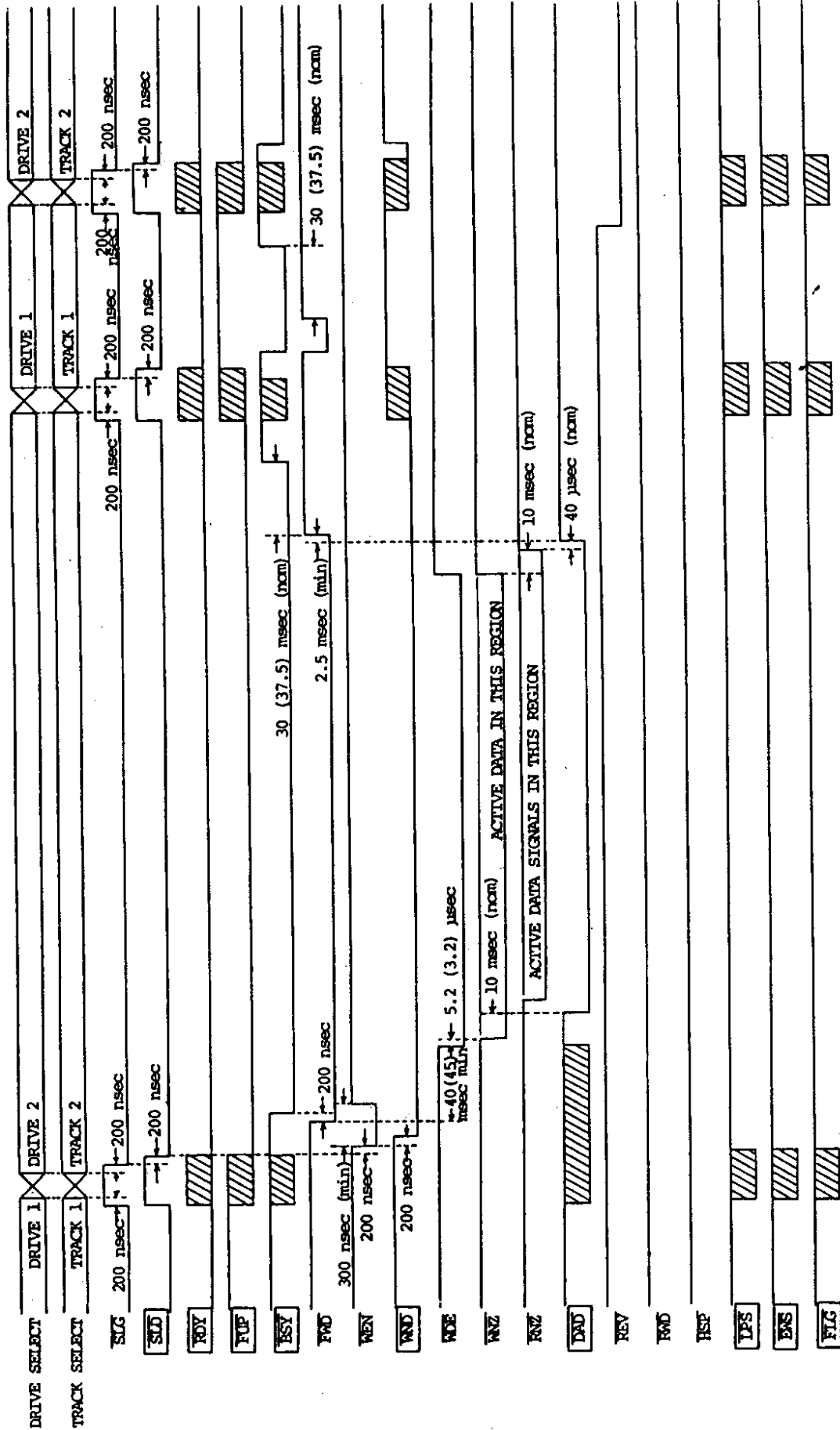


Figure 5.1, Write Timing Diagram

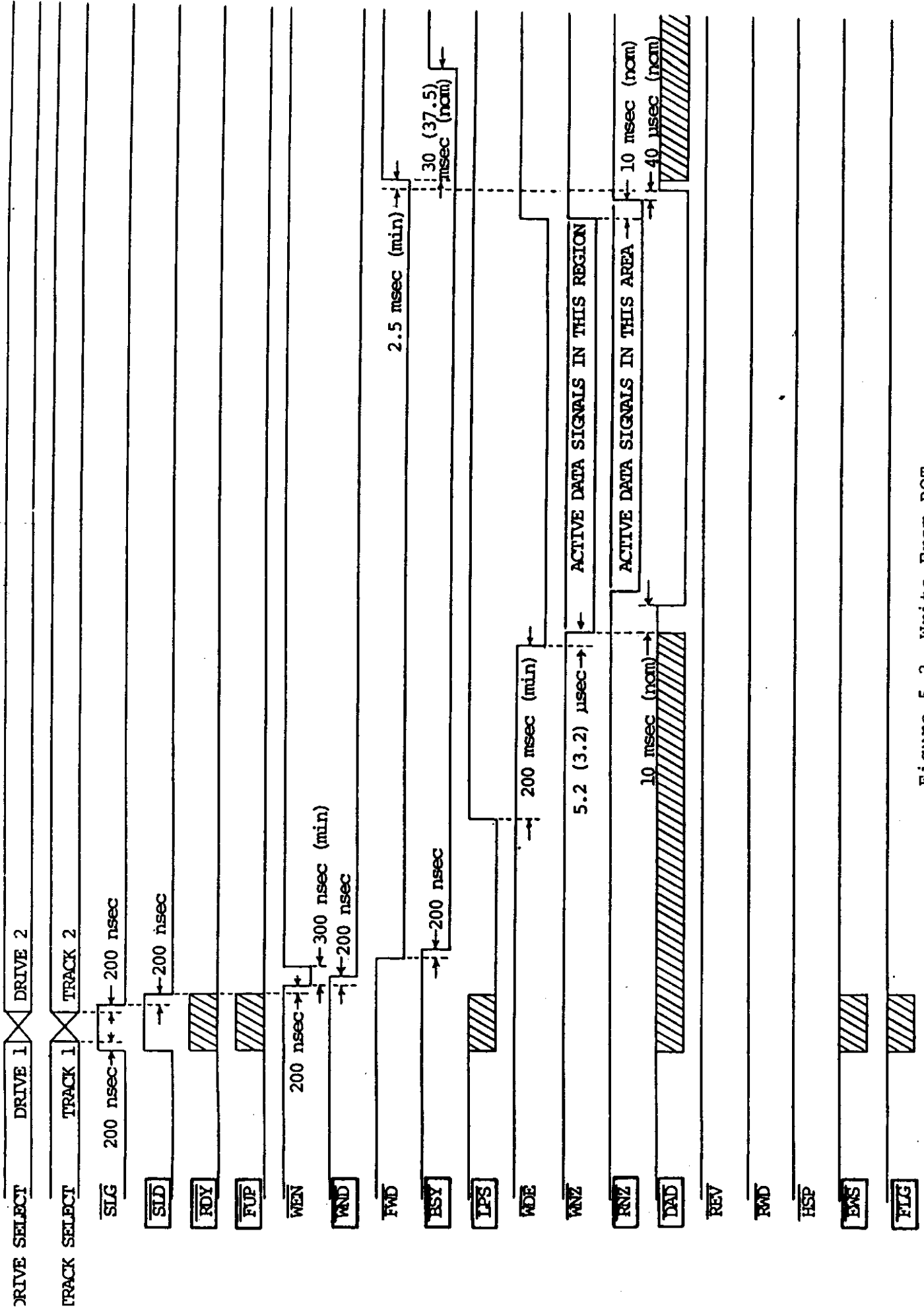


Figure 5.2, Write From BOT

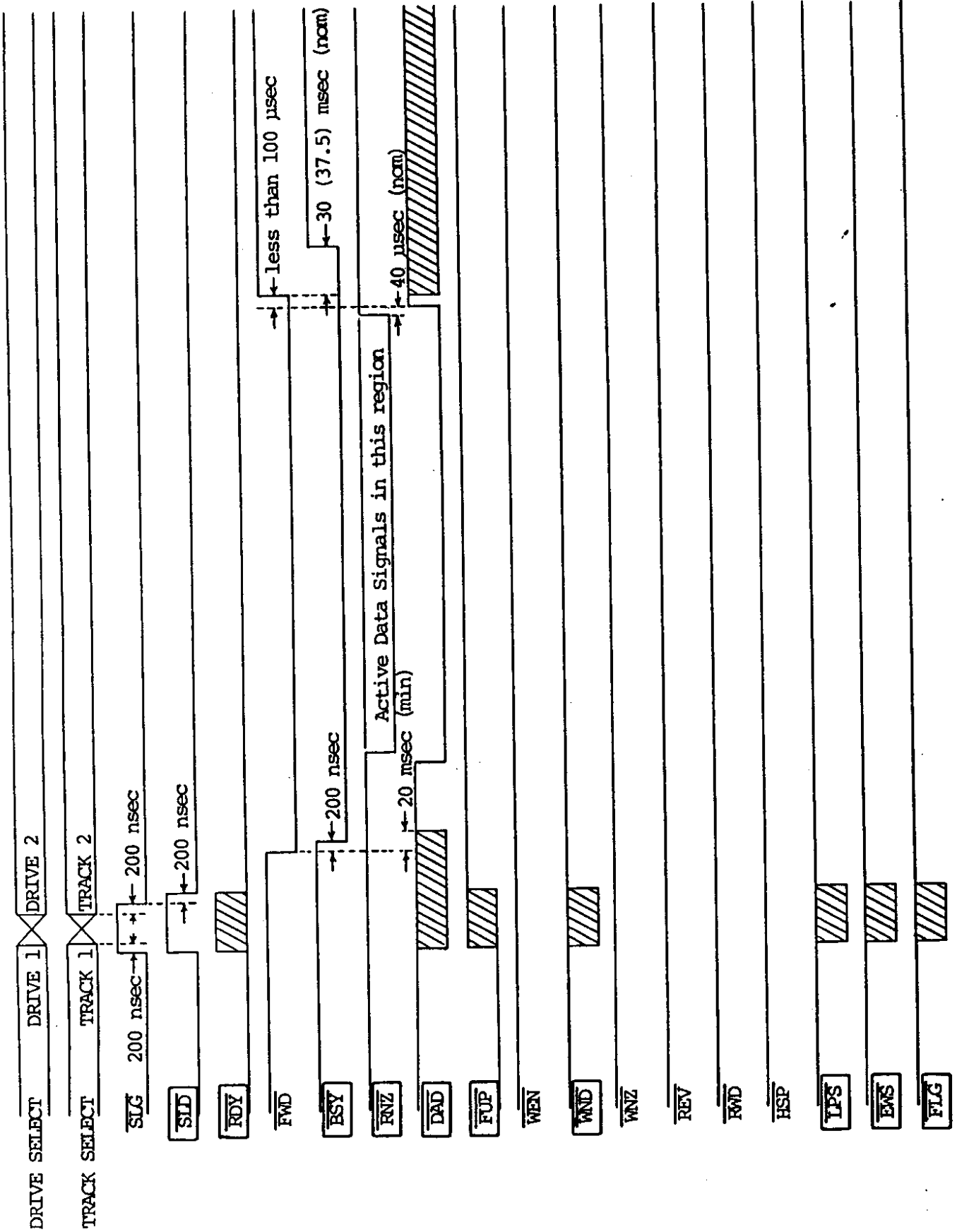


Figure 5.3, Read Timing Diagram

DRIVE SELECT (stable)

TRACK SELECT (stable)

SLG

SLD

RDY

HSP

FWD

BSY

DAD

RNZ

WEN

WND

WNZ

FUP

RWD

IPS

EMS

FLG

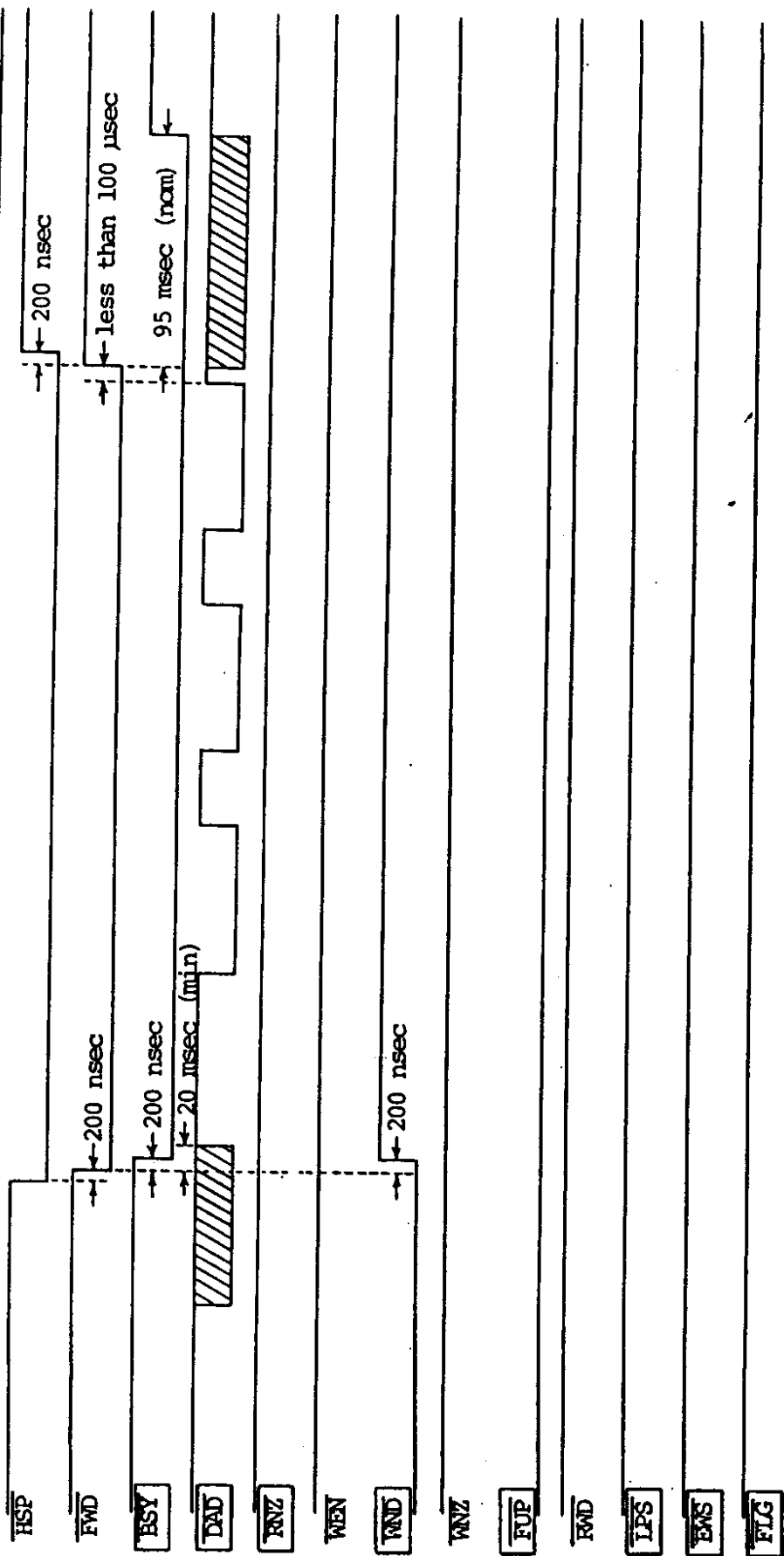


Figure 5.4, High Speed Search Operation

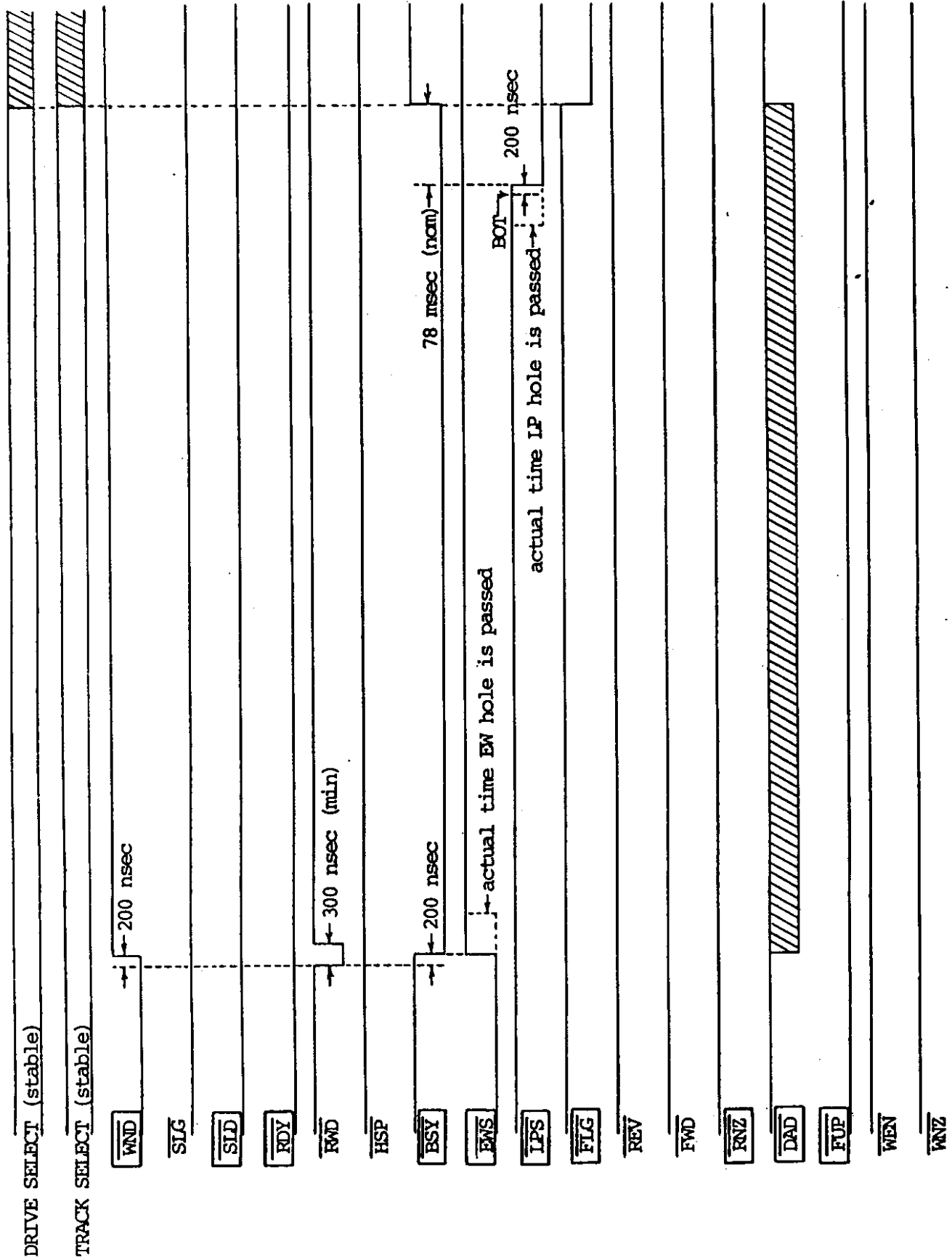


Figure 5.5, Rewind From EWS

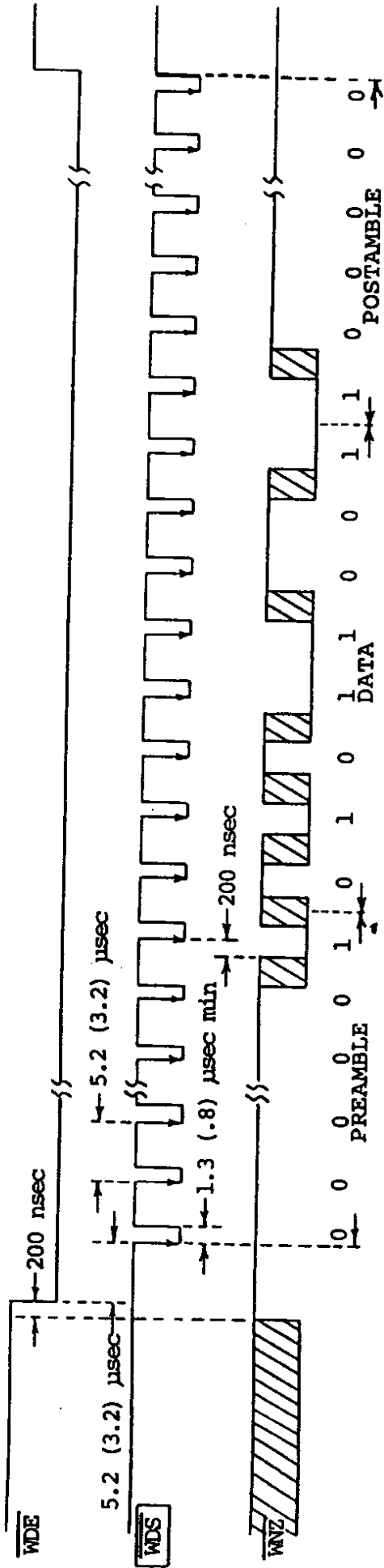


Figure 5.6, Write Waveforms

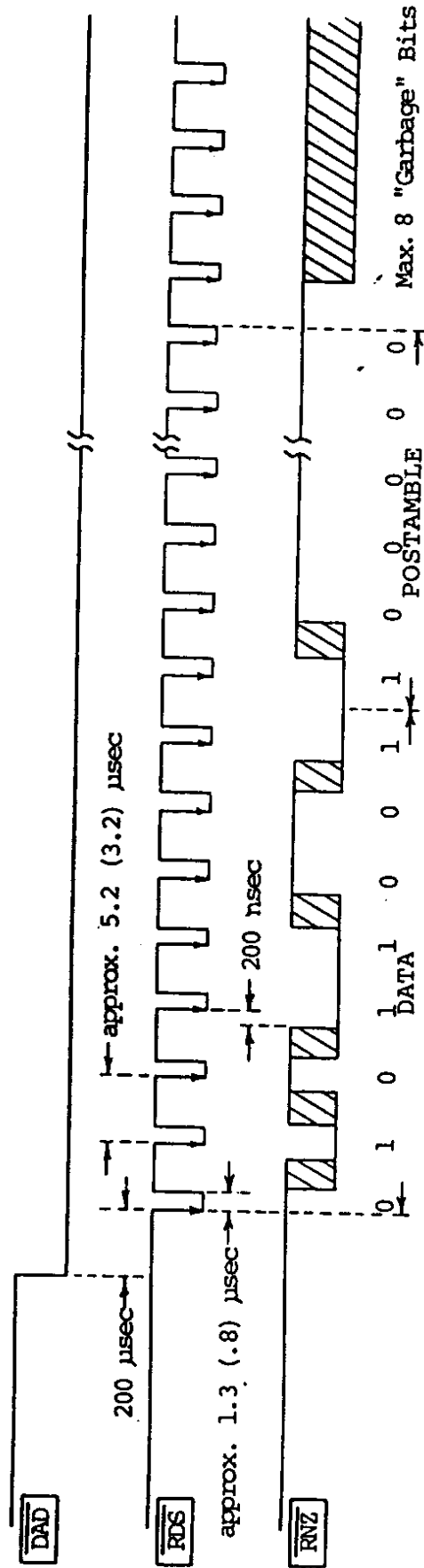


Figure 5.7, Read Waveforms

6) MAINTENANCE AND CALIBRATION

6.1 INTRODUCTION. This chapter describes the maintenance and repair of the Digi-Data 6400 Series Cartridge Drive. It includes procedures for replacing all printed circuit boards and assemblies.

6.2 MAINTENANCE. The only routine maintenance required by the Cartridge Drive is head cleaning. The procedure below should be performed after every eight hours of system use or every week if the system is not used frequently. The correct procedure is:

- 1) Remove the cartridge.
- 2) Moisten a cotton swab with isopropyl alcohol or a commercial head cleaning solvent. Excessive liquid is not required.

CAUTION DO NOT use carbon tetrachloride or any abrasive. Use of these will damage the head.

- 3) Clean the tape head thoroughly using firm vertical and horizontal strokes.
- 4) Once cleaned, allow a few seconds for the solvent to evaporate before loading a cartridge.

6.3 BOARD & ASSEMBLY REPLACEMENT PROCEDURES.

6.3.1 ENTIRE DRIVE. Before any of the replacement procedures can be performed, the drive must be removed from its housing.

- 1) Disconnect the AC power source.

WARNING! Power supply components in the cartridge drive housing can pose a shock hazard if the AC power is not removed.

- 2) Remove the four screws holding the drive to its housing.
- 3) Carefully withdraw the drive as far as possible. If there is an Options Connector on the Control Board, note its orientation and remove it. Then remove the power connector (JP) and the interface cable from the drive.
- 4) Lift the drive the rest of the way out.
- 5) To replace the drive, reverse the above procedures. No calibration is necessary.

6.3.2 CONTROL BOARD.

- 1) If the Control Board is being replaced remove the cable connecting the Control Board to the Servo Board. Pry it off from the ends using a small screwdriver.
- 2) Remove the screws holding the Control Board to the drive. Detach it from the plastic retainers at the front of the drive by squeezing the ears of the retainers, and lift it out of the drive.
- 3) To replace, snap the Control Board onto the plastic retainers and tighten the screws. Reattach the cable. No calibration is necessary.

CAUTION Do not overtighten the screws or they will strip the nylon spacers.

6.3.3 SERVO BOARD.

- 1) Remove the Control Board.
- 2) Remove all connectors from the back of the Servo Board.
- 3) Unscrew the nylon spacers holding the Servo Board to the frame and the two screws holding the heatsink to the baseplate. Lift the board out slightly and detach the motor connector. Remove the board.
- 4) To replace the board, reverse the above procedure. If a different board has been installed it will be necessary to perform a complete calibration. See section 6.4 for procedures.

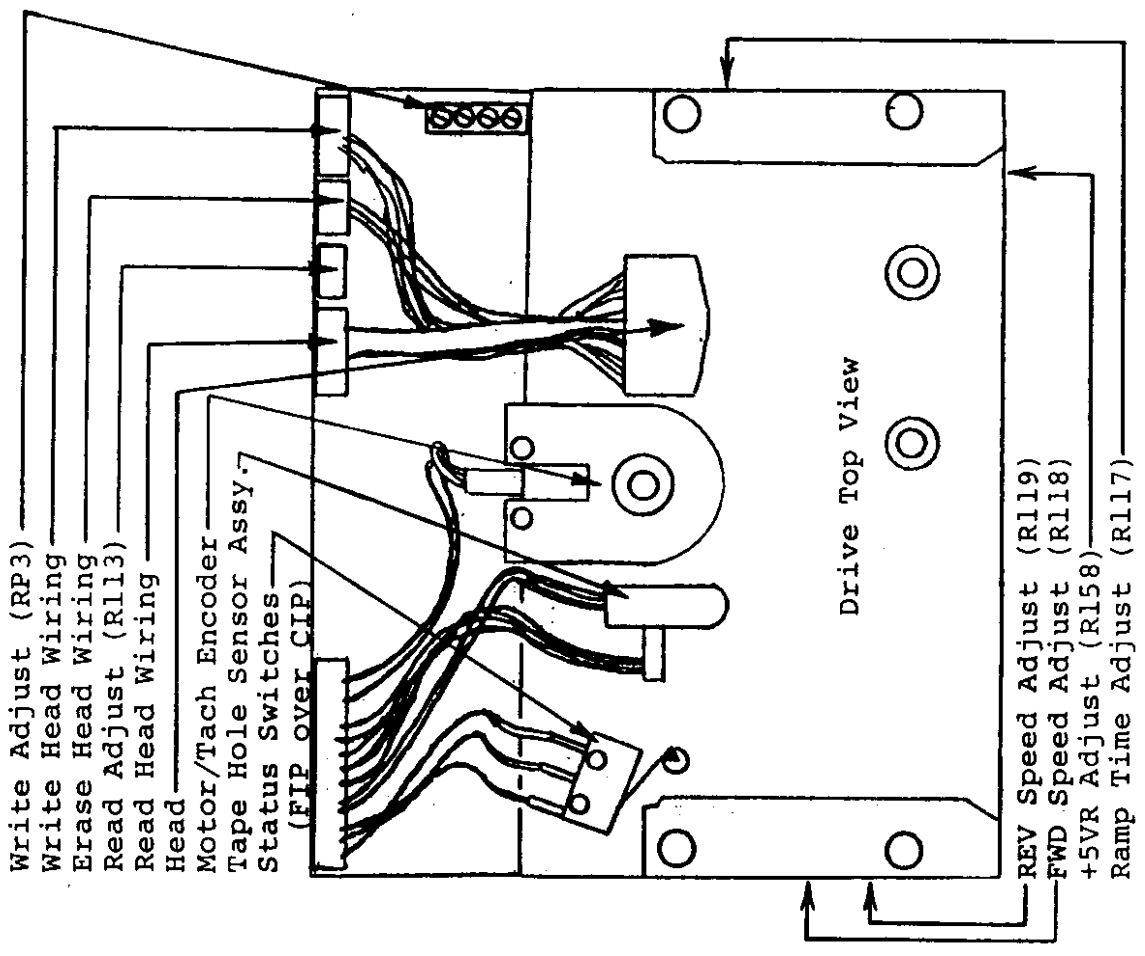
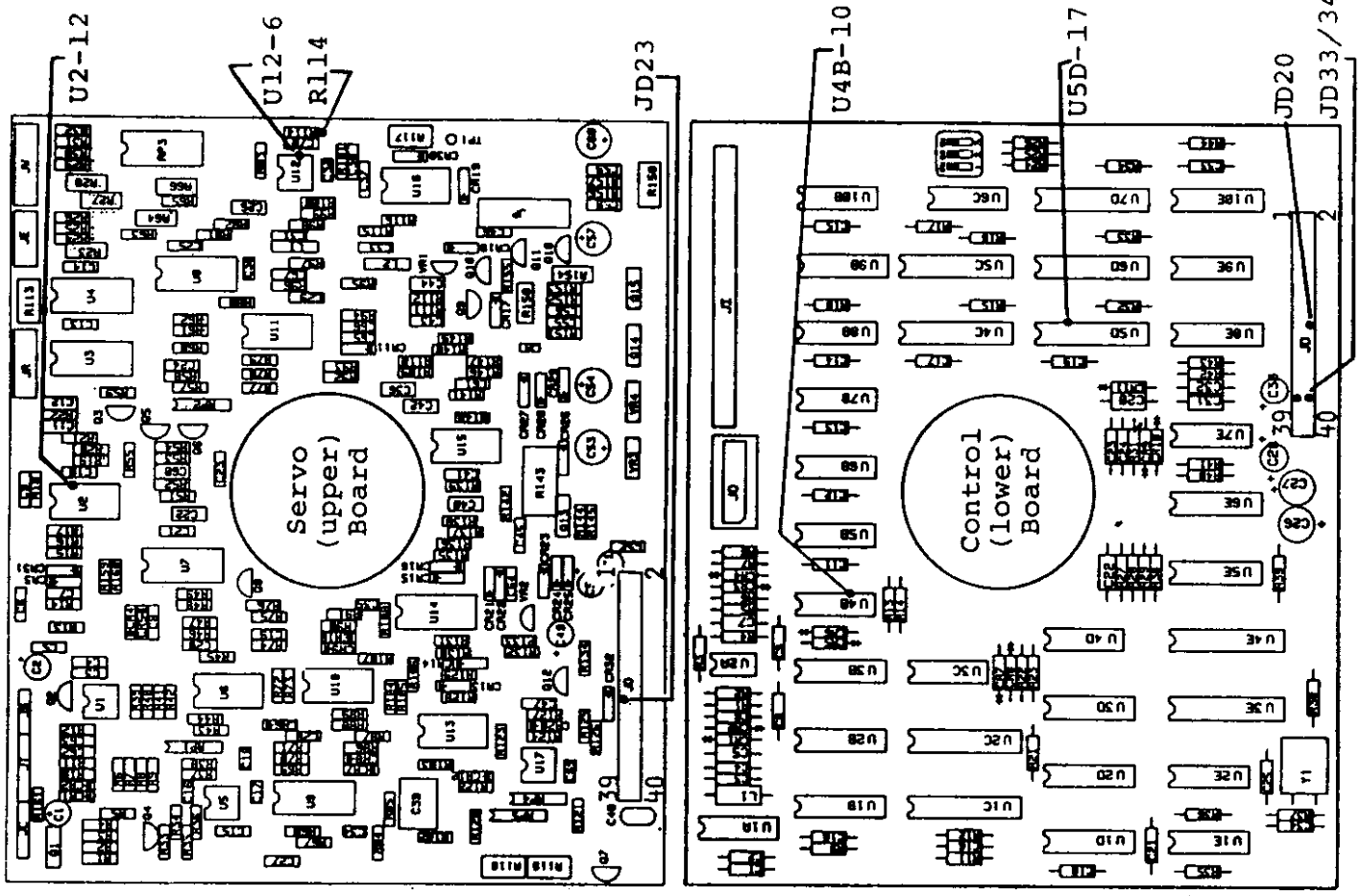


Figure 6.1, Parts Locations

6.3.4 TAPE HOLE SENSOR ASSEMBLY.

- 1) Loosen (do not remove) the screw holding the Tape Hole Sensor Assembly in place. Detach the connector from the Servo Board. Remove the sensor assembly.
- 2) To replace, place the sensor assembly in position and snug (do not tighten) the screw. Insert a cartridge into the drive to act as a guide. Position the sensor assembly so that the overhanging portion is centered over the window in the cartridge (front edge of the assembly will be parallel to the front edge of the cartridge). Hold it in this position and tighten the screw.
- 3) Replace the connector. No calibration is necessary.

6.3.5 STATUS (CIP/FIP) SWITCH ASSEMBLY

- 1) Remove the connector from the Servo Board. Unscrew the two screws from the CIP and FIP switches, being very careful not to lose the washers and nuts underneath the mounting plate. Remove the two switches.
- 2) To replace, place the CIP and FIP switches in position (actuators to the left) and put the screws in place. Carefully replace the washers and nuts and tighten.

CAUTION Do not overtighten these screws or the plastic switches will break.

- 3) Replace the connector. Insert a cartridge and check that both switches can be activated. Loosen the screws and adjust the switches position if necessary. No calibration is necessary.

6.3.6 MOTOR/TACH ENCODER ASSEMBLY.

- 1) Remove the printed circuit boards.
- 2) Unhook the spring. Loosen the four screws holding the motor gimbals. Rock the gimbals back out of the sockets and remove the Motor/Encoder Assembly. NOTE: The gimbals do not have to be removed entirely; simply slide them out of the way.
- 3) To replace the Motor/Encoder place it into position. Slide the gimbals into place and tighten the four screws. Replace the spring. Replace the printed circuit boards.
- 4) It will be necessary to adjust the tape speed and ramp times. See section 6.4 for procedures.

6.3.7 HEAD.

- 1) Remove the printed circuit boards.
- 2) Remove the two screws holding the head in place from the underside of the top plate. Retain all hardware and plastic shims from under the head. Remove the head.
- 3) To replace the head, put it into place square to the mounting plate and replace the hardware. The Read and Write portions of the head should extend equally into the tape path. Check that the head body is not shorted to the chassis. Replace all printed circuit boards.
- 4) It will be necessary to calibrate the Read Amplifier and the Write Circuitry to the new head. See section 6.4 for details.

6.4 CALIBRATION PROCEDURES.

WARNING! While there are no hazardous voltages in the drive itself, performing the following may place the technician near dangerous AC power supply components. Read the manual for the system which contains the cartridge drive before proceeding.

ADJUSTMENT: +5 VR LOCATION: R158 TEST POINT: Control Board, JD33/34

PROCEDURE: Adjust R158 to obtain 5.00 ±.05 volts.

ADJUSTMENT: FWD Speed LOCATION: R118 TEST POINT: Control Board, U4B pin 10

PROCEDURE: Install a Master Speed Tape (96.000 KHz signal) in the drive.

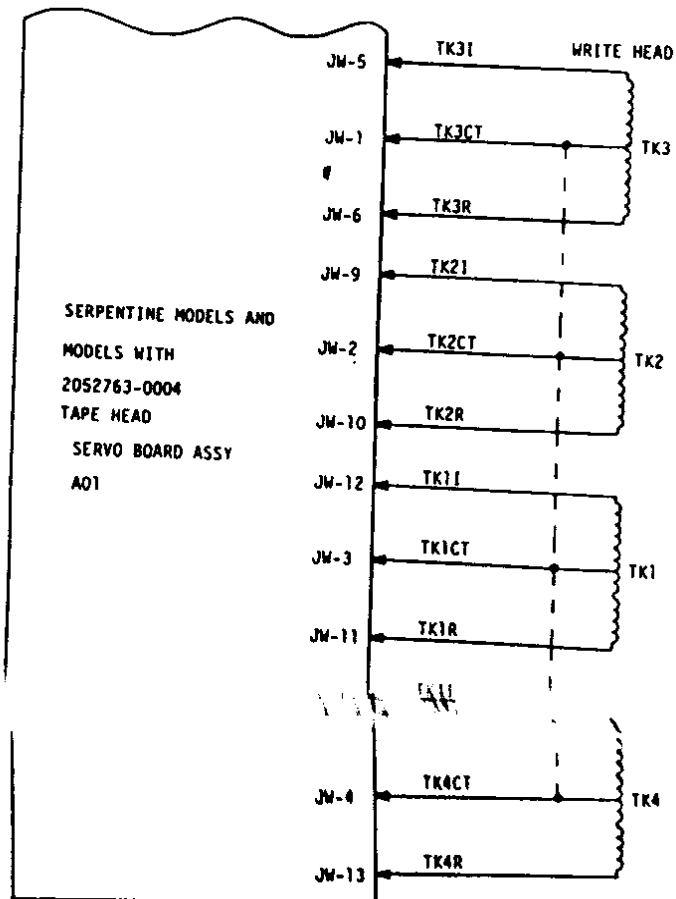
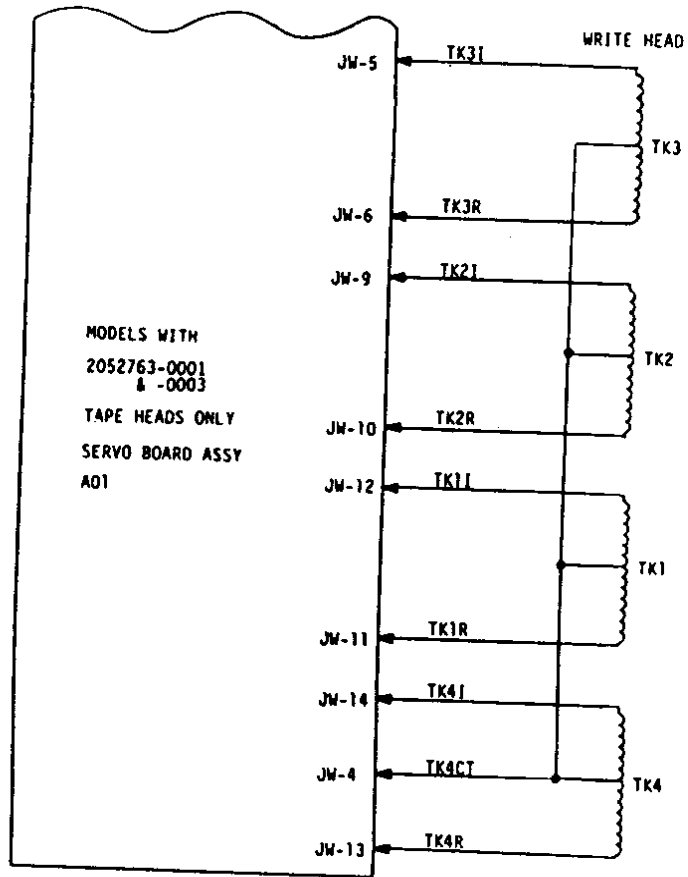
Issue a FWD command to the drive.

Monitoring U4B pin 10 with a frequency meter, adjust R118 for 96 KHz ±1% (±960 Hz).

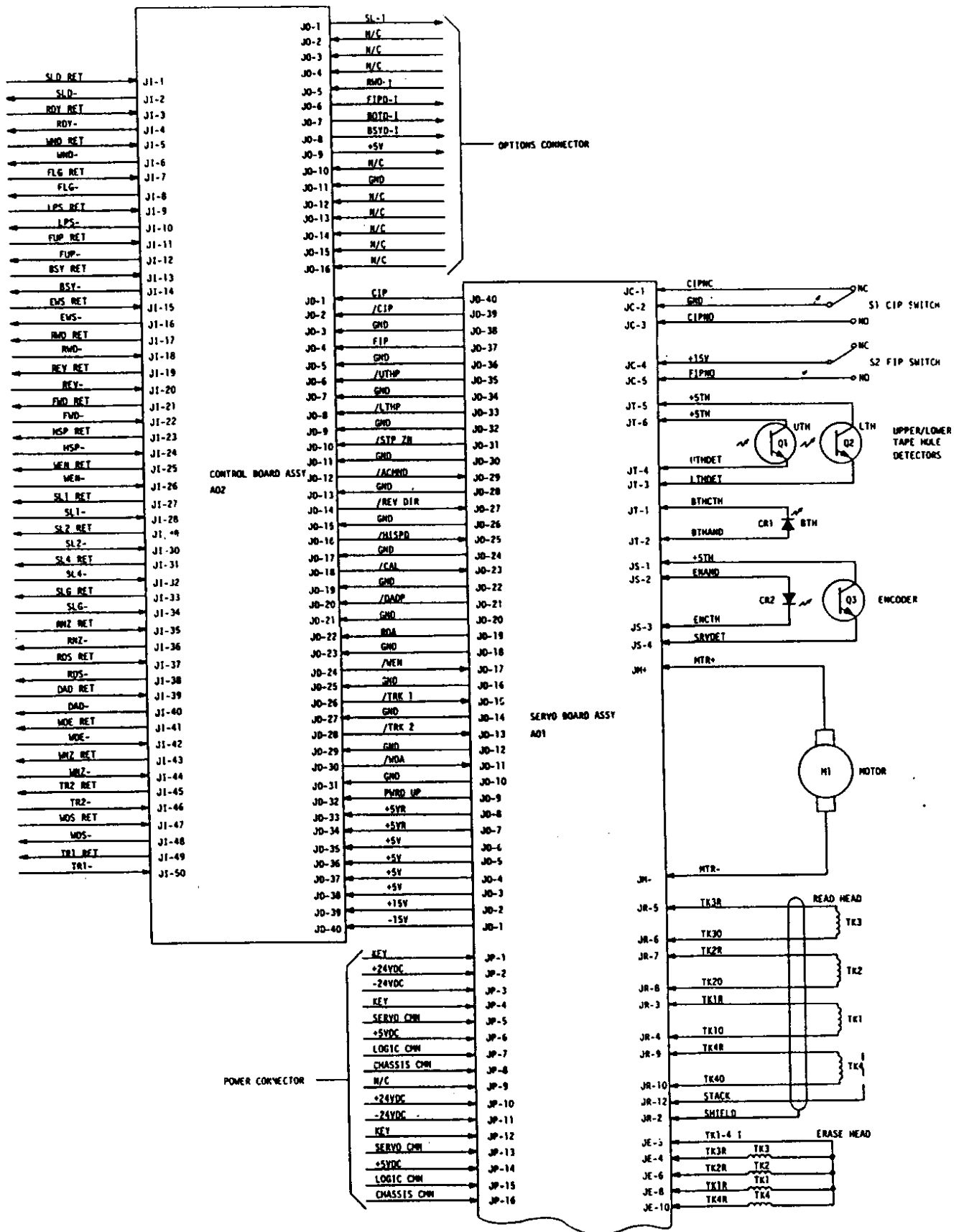
Make only full passes of the tape to keep tape tension controlled and select track 1 or 2 (an inside track) for the most reliable readings.

APPENDIX - APPLICATION NOTES

- A1 Cartridges often lose tape tension during shipment, causing tape slippage and data errors. When using a cartridge for the first time or after it has been in storage or has been mishandled (jarring, etc.) retension the tape by performing a high speed forward to EOT and then rewinding to BOT.
- A2 Shuttling operations and Write-Backspace-Read operations over a single record are not recommended anywhere on the cartridge since they tend to degrade data reliability by loosening tape. If tape tension drops, any deformity in the tape itself (slight wrinkles, bowing, tape hole blemishes cf. Note A3, etc.) will pull the tape away from the head, causing errors. Maintaining tension prevents the tape from pulling away from the head and eliminates these errors. Note A4 gives the recommended write check/error correction procedure.
- A3 The BOT and EOT holes on some cartridges may cause deformities at the beginning of track 3 and at the beginning and end of track 4. Since there is a higher incidence of errors in these zones when the tape is not properly tensioned (cf. A2 above), be especially careful to maintain tape tension while performing any type of error correction routine in these regions. Note A4 gives the recommended procedure write check/error correction procedure.
- A4 To find and correct write errors the following procedure is recommended.
- (1) Perform a read-while-write error check.
 - (2) If any errors are found, finish writing the record. Backspace 5 to 10 records and then read forward. The controller must know where it is in the data. Be careful not to simply backspace over an incorrectly written record and attempt to rewrite; if a dropout occurred, DAD will go false in the middle of the record, giving the controller a false indication of its location in the data, making it all but impossible to correct the write error, aside from possibly losing tape tension (cf. Note A2 above). Backspacing several records avoids the tension problem, and reading forward after the backspace allows the controller to "find its place" in the data so that it can rewrite the entire incorrect record.
 - (3) At the beginning of the record containing the error, rewrite the entire record with an extended interrecord gap to skip over the bad portion of tape.
- A5 Cartridges have ferromagnetic guide pins which may become magnetized in the presence of strong magnetic fields. Data written on a tape with magnetized pins will be degraded as it moves back and forth and passes over those pins. If any possibility exists that unused cartridges have been subjected to a strong magnetic field, it is recommended that they be degaussed completely prior to recording data on them.



Cartridge Drive Schematic: Write Head



Cartridge Drive Schematic

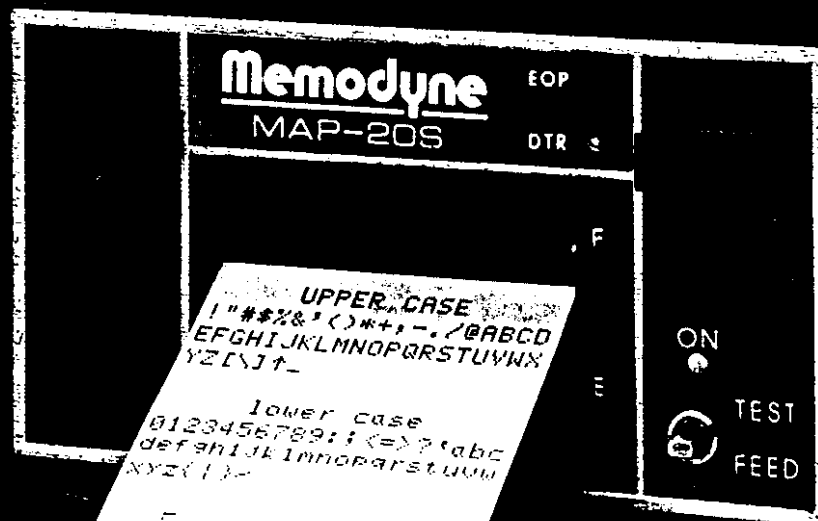


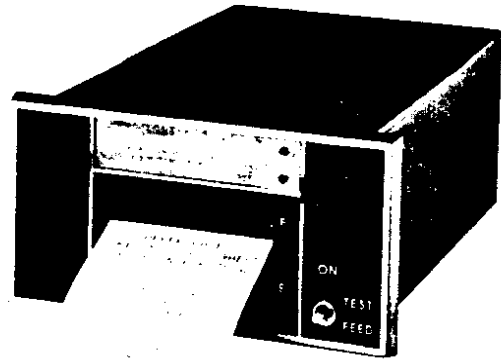
Memodyne
CORPORATION

Subsidiary of Computer Products Inc.

Map-20S Miniature Serial Input-20 Column Alphanumeric-Thermal Printer

- Simple 2-wire data input
- Full 96 character print set
- Quiet inkless thermal printing
- Programmable controls
- Weighs only 4.2 lbs.
- Built-in self test program
- Complete interface electronics for isolated 20mA current loop and RS 232 C





INTRODUCTION

MEMODYNE'S MAP-20S is a miniature, panel-mounting alphanumeric printer utilizing quiet, non-impact thermal printing for low cost display and instrumentation applications. The MAP-20S (MEMODYNE ALPHANUMERIC PRINTER) features 20-column printing in a self contained housing including complete control and interface electronics with AC power supply.

The miniature size of the MAP-20S lends itself to a host of new applications.

With outline dimensions of 4.44W x 2.75H x 7.75D in. (113x70x197mm) to the rear fuseholder excluding front panel, the MAP-20S uses just 95 cubic inches of space and weighs under 4.2 pounds (1.9kg). The small size is made possible by using an internal dedicated microprocessor for control, timing, character generation, printhead drive and motor stepping and as a UART.

The MAP-20S is expressly designed for smart analytical instruments, process control monitors, industrial data loggers, security systems, hotel management dispatchers, assembly line tally systems, data acquisition systems, aircraft and vehicle systems, telephone and data communications loggers and traffic, environmental and noise data loggers. In addition, the MAP-20S is an ideal, low cost alphanumeric printer for most microprocessor development systems.

The MAP-20S is a self-contained printer systems module and does not require separately-mounted interface electronics, power supplies and bulky cabling.

DESCRIPTION

The MAP-20S prints the full ASCII character set of upper and lower case letters, numerals, punctuation, etc. in 20 column lines across the paper. The internal control electronics of the MAP-20S offer special OEM programming features which would be impossible with an ordinary print mechanism. These features are either data-word or pin-selected and include:

Print Direction, Buffer Mode, Character Size, Form Feed, Vertical Tab, Horizontal Tab, Backspace, Carriage Return, and Line Feed.

The serial MAP-20S simplifies external wiring to a minimum by requiring only 2 wires for the 20 mA current loop interface. The optoisolation feature protects against common mode noise and ground loop problems.

The MAP-20S accepts serial input data in ASCII format. Both 20mA loop and RS-232-C electrical levels may be accepted on separate input pins. One character line (up to 20 characters) of input data is stored in an internal input register. Data input must then be halted briefly while the MAP-20S drives the thermal printhead and advances one line. Data is accepted at pin-selectable data rates from 75 to 9600 baud.

The RS-232-C input includes a Data Terminal Ready standard control output to synchronize start-stop data loading from remote sources.

FEATURES

- Needs only 2 wires to interface, simplifies input connections to any computer serial port.
- Includes all internal serial data and drive electronics and AC power supply. No extra electronics required. No bulky additional chassis or cables.
- Miniature 20-column alphanumeric panel-mount thermal printer.
- Internal microprocessor and UART includes 1-line, 20 character input buffer.
- Internal or external BAUD rate clock.
- Serial 20 mA TTY current loop input is current direction independent and optoisolated to 300V_{RMS}. Eliminates ground loop noise problems. Permits positioning of the printer hundreds of feet from a computer.
- Standard RS-232-C connector also included.
- 4.2-pound featherweight, 115 lines per min (2 lines/sec) at high baud rates.
- Jumper or logic selected baud rate (75 to 9600) at any bit character length (9, 10, or 11).
- Jumper, logic, or character-selected (SO/SI) EXTENDED CHARACTERS.
- Jumper or logic-selected inverted (TEXT) printing or normal (LISTER) printing.
- Includes switchable dual 115.230 VAC power supply; OEM's stock one version, choice of line cords.
- Electronic End of Paper sensing allows printing to the last inch of paper.
- Internal self test program prints entire character set and is initiated from the front panel switch.
- 5V, 1/2A regulated DC power supply available for use on user's external electronics.

APPLICATIONS — USE THE MAP-20S FOR:

- Miniature hard copy printer for medical systems, analytical instruments and diagnostic testers.
- Remote Slave Printer Terminal hundreds of feet from data source.
- Multiple-station, daisy-chained message repeater using 2-wire interconnects.
- Portable test and measurement instrumentation for laboratory or field use.
- Serial interface data logger or industrial data acquisition system with terminal at operator's station remote from hazardous process.

SPECIFICATIONS

GENERAL

The MAP-20S prints alphanumeric information in 20 character columns on an internal roll of paper from externally supplied ASCII encoded characters. The MAP-20S receives both industry standard 20 milliamp current loop levels and RS-232-C voltage levels.

The MAP-20S prints all upper and lower case ASCII letters, numbers, punctuation, and special symbols shown in ANS X3 4-1977 in a 5-column by 7-row dot matrix. The printing is accomplished using a dot-line, thick-film, non-impact ceramic thermal printhead by sequentially printing each 20 character-row of the character matrix. After each character-row has been printed, a stepper motor advances the paper. After the entire character-line has been printed, the paper is advanced 4 more character-row spaces, allowing the printed character-line to be immediately viewed.

The printhead design is self-cleaning. Periodic cleaning of the mechanism, printhead, and drive roller with isopropyl alcohol may be required. Cleaning is suggested for dirt accumulation depending on operating conditions.

WEIGHT with full paper roll 4.2 lb
1.9 kg

DIMENSIONS

Outline (note 1) 4.44 x 2.75 x 7.00 in.
112.8 x 69.9 x 177.8 mm
Front Panel 5.25 x 2.81 in.
133.4 x 71.4 mm
Front Panel 4.50 x 2.78 in.
Cutout 114.3 x 70.6 mm

ABSOLUTE MAXIMUM RATINGS

Temperature Range (T_A)
Operating 0 to 50 °C
Storage (note 2) -25 to +85 °C
Relative Humidity Range (RH)
noncondensing 20 to 90%
Input line
Voltage Range (V_i) 115V 105 to 130 V_{RMS}
230V 210 to 260 V_{RMS}
Frequency Range (F_i) 47 to 440 Hz
Voltage On Any Pin (with respect to ground)
RX RS232, RX TIMING
DATA TERMINAL READY -30 to +30V
RX ILOOP
Maximum common mode 300V
All Other Pins -0.7 to +6.0V
Current Through RX ILOOP 50 mA

CHARACTERISTICS

$T_A = 25^\circ\text{C}$ RH=50% $V_i = 115\text{V}$
 $F_i = 60\text{Hz}$ Data Rate=9600 baud

PARAMETER	CONDITIONS	LIMITS			UNITS
		MINIMUM	TYPICAL	MAXIMUM	
Print Rate					
Normal Size Char.		—	110	240	lines/min
Extended Size Char.		—	75	175	lines/min
Line Density					
Normal Size Char.		—	5.3	—	lines/in.
		—	0.21	—	lines/mm
Extended Size Char.		—	3.4	—	lines/in.
		—	0.13	—	lines/mm
Data Capacity					
Normal Size Char.		1.0 x 10 ⁴	—	—	lines
		2.0 x 10 ⁵	—	—	characters
Extended Size Char.		6.5 x 10 ³	—	—	lines
		1.4 x 10 ⁴	—	—	characters
Character Size					
Height	Normal	—	0.115	—	in.
	Normal	—	2.92	—	mm
	Extended	—	0.225	—	in.
	Extended	—	5.72	—	mm
Width		—	0.080	—	in.
		—	2.03	—	mm
Power Consumption					
Average	Idle	—	4.3	—	W
	Printing	—	12	—	W
	Peak	—	65	—	W
Output Voltage					
Input Register Full					
Low Level, V_{OL}	$I_{OL} = 1.8\text{mA}$	—	—	0.4	V
High Level, V_{OH}	$I_{OH} = -100\mu\text{A}$	2.4	—	—	V
End of Paper					
Low Level, V_{OL}	$I_{OL} = 1.8\text{mA}$	—	—	0.8	V
High Level, V_{OH}	$I_{OH} = -100\mu\text{A}$	2.4	—	—	V
Data Terminal Ready					
RX Timing					
Low Level, V_{OL}	$R_L = 3\text{Kohm}$	—	—	-5	V
High Level, V_{OH}	$R_L = 3\text{Kohm}$	5	—	—	V
Input Voltage					
All inputs except RX RS232 & RX ILOOP					
Low Level, V_{OL}		—	—	0.8	V
High Level, V_{OH}	(note 3)	2.0	—	—	V
RX RS232					
Mark		-25	—	+0.75	V
Space		1.75	—	25	V
Input Current					
RX ILOOP (pair)	compliance				
Mark	voltage=	10	20	40	mA
Space	5.0V	—	0	2	mA
Power Supply					
Output Voltage, V_O	$I_O = 0$ to 0.5A	4.75	5.0	5.25	V
Line Regulation, V_O					
over full V_i range	$I_O = 0.25\text{A}$	10	1.0	—	mV
Load Regulation, V_O	$I_O = 0$ to 0.5A	50	38	—	mV
Fuse (type 3AG)					
115V Range		—	—	1/2	A SLOW
230V Range		—	—	1/4	A SLOW
Length		—	1.25	—	in.
Diameter		—	0.25	—	in.
Internal Baud Clock	all baud rates				
Error		—	0.5	2	%
Input Register Full					
Pulse Width		—	10	—	μs
Repetition Rate		—	13.3	—	kHz
Print Pulse Width		5.0	—	—	μs
Print Head Life	(note 4)	—	1 x 10 ⁷	—	lines

- notes: 1 Outline dimensions are exclusive of front panel, connector, and fuse.
2 The paper will darken with prolonged storage above 60 °C
3 A high level may be achieved with no connection.
4 Using a random character distribution and Memodyne supplied paper.

I/O SIGNAL DESCRIPTION

CONTROL INPUTS:

NOTE: All printer control inputs contain internal pull-up resistors. A no connection achieves a logic high.

INTERFACE SELECT

Pin 5 (ILOOP/RS232) Input. One LSTTL and one 75489A load with 4.7K pullup resistor.

Interface Select low, is RS232 true. RS232C true, connects the RX RS232C input line to the printer control electronics. Interface Select high is ILOOP true. ILOOP true, connects the RX ILOOP data inputs to the printer control electronics. The state of Interface Select is scanned at power-up and at the end of the self-test sequence.

BAUD CLOCK SOURCE

Pin 6 (EXT/INT) Input. One LSTTL load with 4.7K pullup resistor.

Baud Clock Source low, is INT true. INT true, connects the internal baud rate generator (at a rate determined by Baud Rate Select inputs) to the printer control electronics. Baud Clock Source High is EXT true. EXT true, connects the EXT CLK input to the printer control electronics. The state of Baud Clock Source is scanned at power-up and at the end of the self-test sequence.

CHARACTER LENGTH SELECT

Pin 13 (CB2) Pin 12 (CB1) Pin 11 (CB0) inputs. One LSTTL load with 4.7K pull-up resistor.

The MAP-20S accepts the following character lengths independent of the state of the Character Length Select inputs.

TOTAL # OF BITS	# OF BITS		
	START	DATA	STOP
10	1	8	1
9	1	7	1
10	1	7	2
11	1	8	2

BAUD RATE SELECT

Pin 21 (BS3), Pin 22 (BS2), Pin 23 (BS1), Pin 24 (BS0) Inputs. One LSTTL load with 4.7K pull-up resistor

The Baud Rate Select inputs control the clock rate of the internal baud rate generator according to the following table:

BAUD RATE	1= HIGH 0= LOW			
	BS3	BS2	BS1	BS0
75	0	0	1	1
110	1	1	1	1
150	1	1	1	0
300	1	1	0	1
600	0	1	1	0
1200	1	0	1	1
2400	0	1	1	1
4800	1	0	0	1
9600	1	0	0	0
NONE	ALL OTHER CODES			

The state of Baud Rate Select is scanned at power-up and at the end of the self-test sequence.

CHARACTER SIZE SELECT

Pin 9 (CS0) Pin 8 (CS1) Inputs. One LSTTL load with 4.7K pull-up resistor

The Character Size Select inputs control the size of the printed character according to the following table:

1= HIGH 0= LOW		CHARACTER SIZE
CS1	CS0	
0	0	CONTROL CODE SELECTED*
0	1	NORMAL
1	0	NORMAL
1	1	EXTENDED

*SO (0E Hex-CTRL N) To extended sized characters
SI (0F Hex-CTRL O) To normal sized characters
The initial state is normal sized characters

A normal size character is 7 dot lines high. An extended size character is 13 dot lines high. The full 96-character print set (both upper and lower case) may be printed normal size or extended size. The state of the Character Size Select input is scanned after each character is received and DTR is true. Character size may change on a character by character basis. Extended size and normal size characters may be mixed on a single line.

PRINT DIRECTION

Pin 14 (TEXT/LISTER). One MOS input with 6K pull-up resistor.

Print Direction high, is TEXT true. With TEXT true, characters appear inverted when viewed at the front panel. When viewing a page of text mode printing, the last line printed is at the bottom of the page. Print Direction low, is LISTER true. Lister true places the printer in the list mode. With LISTER true, characters appear non-inverted when viewed at the front panel. When viewing a page of list mode printing, the last line printed is at the top of the page. Print Direction is scanned after the first character of a print line is received and DTR is true. The print direction will only change on a line by line basis.

BUFFER MODE

Pin 15 (LINE BUFFERED/SINGLE CHARACTER PRINTING). One MOS input with 6K pull-up resistor.

Buffer Mode high is LINE BUFFERED true. With LINE BUFFERED TRUE, data characters are printed a line at a time after storing them in the input line buffer. Characters are not printed as they are received. Buffer Mode low is SINGLE CHARACTER PRINTING true. With SINGLE CHARACTER PRINTING true, data characters are printed as they are received, as in keyboard echo applications. Buffer Mode is scanned after the first character of a print line is received and DTR is true. The buffer mode will only change on a line by line basis.

AUXILIARY PRINT

Pin 25 (PRINT) active low. One pseudo TTL input with 4.7K pullup resistor.

Print true, prints the characters stored in the line buffer and advances the paper one character line. Holding PRINT active, acts as a remote paper feed after printing one line. When printing a line, PRINT must go inactive before DTR becomes active to insure that a remote paper feed will not occur.

STATUS OUTPUTS:

END OF PAPER

Pin 16 (EOP) Output, active low. A darlington transistor with 4.7K pull-up resistor and one LSTTL load. EOP active indicates that the paper is within 1 inch of exhaustion. The printer is disabled when EOP becomes active.

INPUT REGISTER FULL

Pin 2 (IRF) Output, active low. An MOS output with 6K pull-up resistor.

The IRF pulse train indicates that the line buffer is full and any additional printable data characters will be ignored. It begins once the 20th character is placed in the line buffer and continues until:

- 1: the line is printed
- 2: the buffer is reset with the Delete (Del 7F Hex) command
- 3: a character is removed from the buffer with the back-space (BS 08 Hex-CTRL H) command.

An IRF pulse is issued following the receipt of a carriage return (CR 0D Hex-CTRL M). IRF may be wired directly to the PRINT input to automatically initiate printing upon receipt of the 20th character in a line.

DATA TERMINAL READY

Pin 20 (DTR) Output, active high. One RS-232-C transmitter. DTR true may be used to control switching the user's data communication equipment to the RX DATA RS232 input. DTR inactive, indicates the printer is busy and is unable to receive additional data or commands. The user's data communication equipment must stop data transmission after DTR goes false. The character in transmission may be completed.

DATA INPUTS:

RX ILOOP

Pins 17 and 18 (RX ILOOP) Input active when 20 mA current flowing. A rectified optoisolated current loop receiver.

Serial asynchronous data input selected when Interface Select is high. The baud rate is controlled by Baud Rate Select inputs.

RX RS232

Pin 3 (RX RS232) Input active low. One RS-232-C receiver. Serial asynchronous input selected when Interface Select is low. The baud rate is controlled by Baud Rate Select inputs.

TIMING IN:

EXTERNAL X16 BAUD CLOCK

Pin 4 (EXT CLK) Input. One LSTTL input with 4.7K pull-up resistor.

EXT CLK is an alternate source for the serial data baud rate. The EXT CLK rate must be 16 times the baud rate (or bits per second). The maximum baud rate is 9600 baud. There is no minimum baud rate. EXT CLK is selected by Baud Clock Source input equal to EXT.

TIMING OUT:

RX TIMING

Pin 19 (RXTIM) output. One RS232C transmitter.

RXTIM, when the Baud Clock Source is EXT, is a copy of EXT X16 Baud Clock.

RXTIM, when the Baud Clock Source is INT, is a X16 baud rate clock.

POWER CONNECTIONS:

VCC

Pin 10 (Vcc)

Regulated +5v DC Power supply with ½A available externally.

LOGIC GROUND

Pin 7 (COM)

Power Supply Return.

CHASSIS GROUND

Pin 1 (CGND)

Chassis Ground Connection

A jumper is provided internally which may be removed to break the connection to the connector.

OPERATING MODES

The MAP-20S is a line printer; it prints a 20 character line of 5-column by 7-row dot matrix characters at once. Each character-line is printed one character-row at a time. In between character-rows, the paper advances one character-row space. To print a character-row, the printhead is energized five times, once for each column in the character-row. If all twenty dots of a particular column and line require no printing, the printer automatically skips to the next column and/or line. This action dramatically increases print rates for sparse lines.

The MAP-20S recognizes 96 of the 128 7-bit ASCII characters as printable. Of the remaining characters, the following characters are interpreted as control characters:

ASCII	HEX 7-bit	KEYBOARD	ACTION
NUL	00	CTRLSHIFT P	Null — do nothing
BS	08	CTRL H	Backspace — Single Character Mode, interpreted as a space; Line Buffered Mode, deletes the previous entry, if the previous entry was the first entry, the buffer is considered empty
HT	09	CTRL I	Horizontal Tab — tab to characters 4, 9, & 15
LF	0A	CTRL J	Line Feed — advance 1 character line, the contents of the input line buffer are not printed, the next data character will be added to the buffer
VT	0B	CTRL K	Vertical Tab — advance 5 character lines, the contents of the input line buffer are not printed, the next data character will be added to the buffer
FF	0C	CTRL L	Form Feed — advance 11 character lines, the contents of the input line buffer are not printed, the next data character will be added to the buffer
CR	0D	CTRL M	Carriage Return — print the contents of the input line buffer
SO	0E	CTRL N	Shift Out — to extended size characters
SI	0F	CTRL O	Shift In — to normal size characters
DEL	7F	DEL	Delete — reset input line buffer, the buffer is considered empty

All other non-printable characters are interpreted as spaces. The data control characters, in conjunction with the I/O programmable control features, make the MAP-20S a versatile panel mountable printer.

There are 3 ways to initiate a print cycle in a MAP-20S. After the data has been loaded into the input buffer the user may:

- 1) send a CR (0D Hex)
- 2) depress the FEED switch
- 3) strobe the Auxiliary Print input

to print the contents of the input buffer. In addition, if one desires that the printer automatically print the contents of the input buffer, when that buffer is full, simply connect the Input Register Full output to the Auxiliary Print input.

HOW TO LOAD PAPER

1 Depress both front panel slide latches and pull the printer mechanism out of the housing until the mechanism stops.

2 Raise the load bracket by pulling it forward until it latches. This automatically lifts the thermal printhead from the paper drive roller.

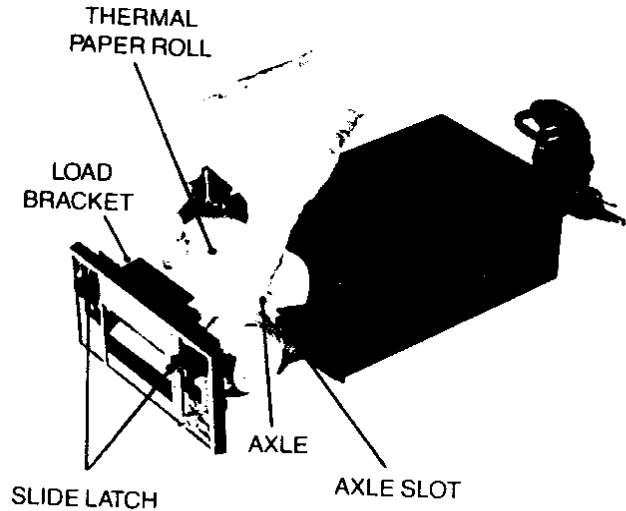
3 Pull the remaining paper out from under the printhead. Grasp the empty paper roll and pull it straight along the axle slot and out of the printer assembly.

4 Slide the paper roll axle out of the used paper roll and insert the axle into a new paper roll. **DO NOT DISCARD AXLE!**

5 Slide the axle (with new paper roll) into the axle slot and seat the axle in the bottom of the slot. Be sure that the paper is threaded from the rear and passes over the paper roll. Paper should be cut straight for easy insertion. Only the outside paper surface is treated for printing.

6 Insert the paper in the slot formed by the paper guide and the printhead until paper appears at the front panel opening. Pull paper through front panel slot, close the load bracket by pressing it downwards, and check that the EOP LED turns off. If not, the paper is not in the proper paper path.

7 Slide the printer mechanism back into the housing until latching both slide latches. Advance the paper by depressing the Feed switch.



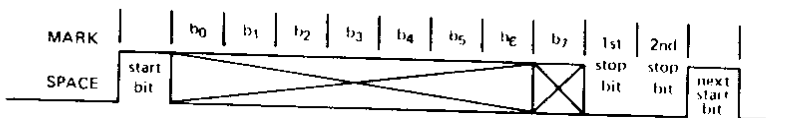
SAMPLE PRINTOUT (ACTUAL SIZE)

```
!"#$%&'()*+,-./0123
456789:;<=>?@ABCDEFGHIJ
HIJKLMNOPQRSTUVWXYZ[
\]^_`abcdef`ehijklmno
pqrstuvwxyz{|}~
@12345678901234567890
@12345678901234567890
@12345678901234567890
@12345678901234567890
```

```
789:;<=>?@ABCDEFGHIJ
89:;<=>?@ABCDEFGHIJK
9:;<=>?@ABCDEFGHIJKL
:;<=>?@ABCDEFGHIJKLM
;<=>?@ABCDEFGHIJKLMN
<=>?@ABCDEFGHIJKLMNO
=>?@ABCDEFGHIJKLMNOP
>?@ABCDEFGHIJKLMNPOQ
?@ABCDEFGHIJKLMNPOQR
```

```
c4c716/'-1+*( ) 075#
570016/'-1+*( ) 1025#
78216/'-1+*( ) 1725#
8716/'-1+*( ) 1875#
0016/'-1+*( ) 1865#
lanoparstuvwxyz{|}~
klanoparstuvwxyz{|}~
jklanoparstuvwxyz{|}
```

TIMING DIAGRAMS

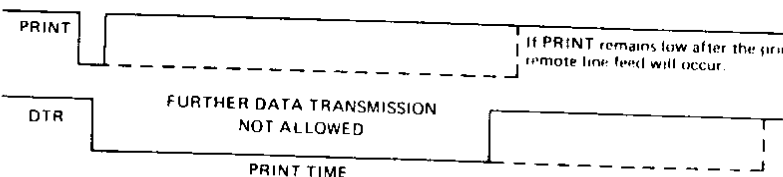
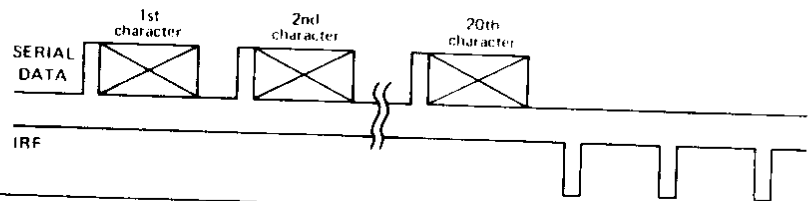


TYPICAL SERIAL DATA

b7 and 2nd stop bit are optional. See I/O signal description of Character Length Select. (Page 4)

TYPICAL CHARACTER LINE TIMING

A single IRF pulse is issued following receipt of a character.



TYPICAL PRINT TIMING

220 to 950 ms depends on number of dot rows with dots to print and character size.

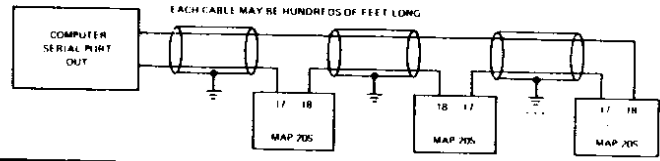
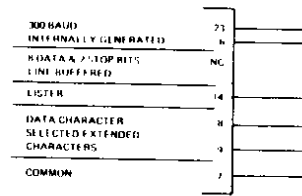
**APPLICATION NOTE 1
USING THE MAP-20S AS A MESSAGE REPEATER**

Several MAP-20S printers may be daisy-chained together using the 20 mA current loop interface to form a multiple-station remote slave terminal network. All the nodes of the network are driven from one computer port with only two wires. Examples of this class of applications include plant security systems where several stations are linked by MAP-20S printers to give periodic hard-copy printout of plant security and time of day information.

The wiring is very simple and noncritical unless very long distances, high electrical noise, or fast baud rates are involved. Each pair MAP-20S RX ILOOP inputs are hooked in series. Since the MAP-20S ILOOP interface is current direction independent, one need not keep track of current polarity. Care should be taken to insure that the sum of the MAP-20S ILOOP interface voltage drops (approximately

3.7V) do not exceed the compliance of the loop driver.

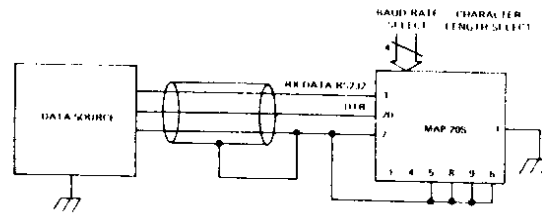
TYPICAL CONNECTOR PROGRAMMING



**APPLICATION NOTE 2
TYPICAL RS-232-C INTERCONNECTION**

When connecting directly to an RS-232-C terminal, the user is cautioned that many programmable features (both inputs and outputs) are included on the MAP-20S's RS-232-C connector. However, some terminals may use these same pins for RS-232-C functions which are not available on or required for the MAP-20S. It may be necessary to internally disconnect these wires before direct connection to such terminals. A CR character must be sent at least every 20 characters to print the contents of the input buffer. Should the user desire an autoprnt after the 20th received data

character, simply connect Pin 2 (IRF) to Pin 25 (Auxiliary Print).



TYPICAL MAP-20S PRINTOUT

One must transmit the following characters to print the sample shown. PRINT (pin 25) was connected to IRF (pin 2) causing an autoprnt after the 20th character in a line. PRINT DIRECTION (pin 16) was connected to ground.

Using the following conventions:

- CR = Carriage Return character
- HT = Horizontal Tab character (CTRL I)
- SO = Shift Out character (CTRL N)
- SI = Shift In character (CTRL O)
- SP = Space

REQUIRED DATA FLOW

- line
- 1 CHHTIMEHTDATEHTSAMPLE
 - 2 toSPcolumnsSP4,9,&,15.
 - 3 SOHTORIZONTALSPSOTSIABSPSO (HT) SICR
- Let PRINT DIRECTION (pin 16) float.
- 4 Selectable SPSOPSIRINTCR
 - 5 SODSIRECTION SPSPINVERTED
 - 6 printing SPforSPSOTEXTSICR
 - 7 applications SPwhereCR
 - 8 last SPlineSPprintedSPis
 - 9 at SPtheSPbottomSPofCR
 - 10 the SPprintoutCR
 - 11 SOSSIZESPSOforSPEMPHASISCR
 - 12 EXTENDEDSPCSIHARACTERCR

PRINTOUT

```

line
12 EXTENDED CHARACTER
11 SIZE FOR EMPHASIS.
10 the printout of
9 to the bottom of
8 it printed but not
7 applications where
6 printing for text
5 DIRECTION, inverted
4 Selectable PRINT
3 HORIZONTAL TAB (HT)
2 to columns 4,9,& 15.
1 CH TIME DATE SAMPLE
  
```

ORDERING INFORMATION:

Model	Description
MAP-20SAC	20 column thermal printer with mating connector, hood and 3 prong U.S. line cord.
MAP-20SEC	Same as above except with VDE CE7-7/7 (DIN 49441) line cord
PT-20B1	Box of 10 rolls of black on white thermal paper. Capacity — 10,000 normal size character lines per roll.

Norman



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